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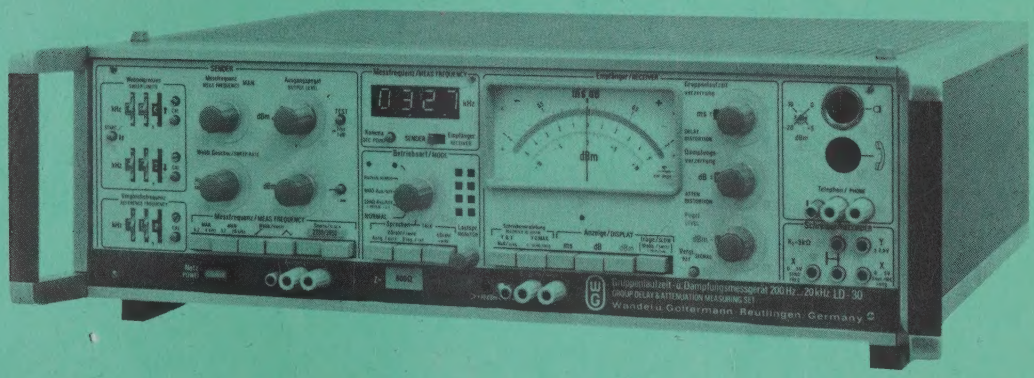
Service Manual



QUALITY ASSURANCE
STANDARDS, CALIBRATION, AND
MAINTENANCE LAB.

Group Delay and Attenuation Measuring Set

LD-30

in the frequency range 200 Hz to 20 kHz

GROUP DELAY AND
ATTENUATION MEASURING SET LD-30

in the frequency range 200 Hz to 20 kHz

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6. PRELIMINARY REMARKS TO SERVICE MANUAL

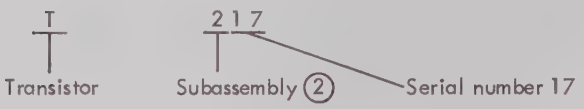
6. PRELIMINARY REMARKS TO SERVICE MANUAL

The following sections 6.1. to 6.5. explain the applied abbreviations, symbols and schematics as used in the "Service Handbook" (Service Manual and Appendix including circuit diagram, layout drawings and component lists).

The tabulated list of applied measurement items in section 6.6. presents the minimum complement of measurement equipment needed for all the measurements suggested in the Service Manual.

6.1. COMPONENT DESIGNATION

The various subassemblies are annotated with an individual number, for instance (2) Input amplifier. Each component located in this subassembly has the number 2 as its first digit. The two subsequent digits define the serial number of the component; for instance, resistor 96 would be R 296, or diode 22 is GI 222 and so on. The prefix letter characterises the type of component.

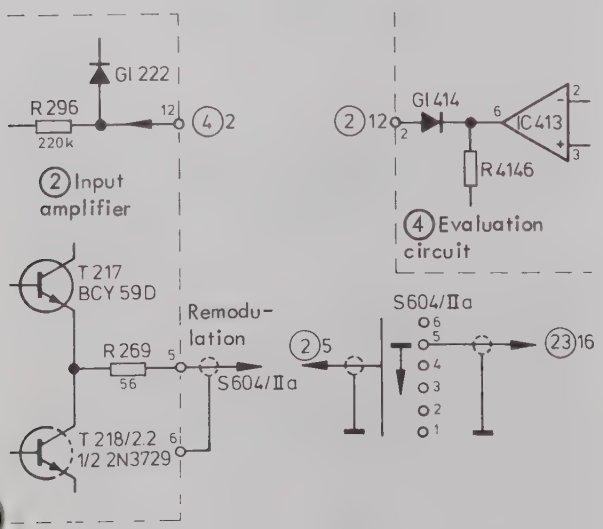


The abbreviations used to designate the components are given in section 6.3.

6.2. INTERCONNECTION BETWEEN SUBASSEMBLIES

Since the circuit diagrams are given separately for each subassembly, it is important that all interconnections are shown clearly. The following drawing explains the method used in this manual.

In the sketch below, point 12 of module (2) is connected to point 2 of module (4), and there is a shielded connection from point 5 of module (2) to switch S 604/IIa of subassembly (6).



6.3. ABBREVIATIONS AND SYMBOLS

In order to achieve greater simplicity, the following abbreviations and symbols have been used in the text and on the circuit diagrams:

6.3.1. Discrete components

Battery	B	
Socket	Bu	
Diode, rectifier	Gl	
Zener diode	G	
LED	Gl	
Thyristor	Gl	
Varactor diode	Gl	
Inductance	L	
Meter	J	
Capacitor	C	
Potentiometer	P	
Quartz crystal	Q	
Relay	Rel	
Relay contact	rel	
Resistor	R	
Thermistor PTC resistor	R	
Switch	S	
Fuse	Si	
Control lamp	SL	
Transistor	T	
Transistor (FET)	T	
Transformer	Ü	

Other important abbreviations:

(2) = subassembly (2) = circuit diagram (2)

691-D = circuit board D

Pkt. 6 = terminal point 6

TP 2303 = test point 2303

6. PRELIMINARY REMARKS TO SERVICE MANUAL

6.3.2. Digital symbols

In the following, some of the most important digital logic switching symbols are given, although the list is not presented as complete.

The two possible states of binary logic are designated "L" (low) and "H" (high). The voltages corresponding to each state are defined as being closer to- ∞ for the "L" range and closer to + ∞ for the "H" range.

6.3.2.1. General symbols

Symbol for negation of an input

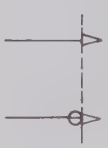
or output:

The dashed line represents the boundary line of the circuit.

Symbol for dynamic input

a) The operation is such that a transition of the input signal from L to H produces an effect similar to a "H" pulse

b) As in a) except operation effective on a H to L transition



Trigger inputs (G inputs)

Static control

operates with a "H" signal — G

operates with a "L" signal — G

one transition control

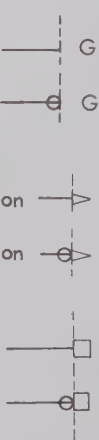
operates with a L - H transition — G

operates with a H - L transition — G

two transition controls

operates with a L-H-L pulse

operates with a H-L-H pulse



Preparatory inputs

E_X = preparing input

X = triggering input

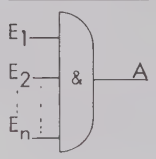
The circuit delivers a "H" pulse when the signal at X transits from L to H, providing a "H" signal is already present at input E_X.

Same as above However, operative when signal at X input transits from H to L.

Note: Any storage time is to be noted (E_X) !

6.3.2.2. Digital signal gates

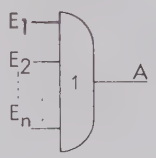
The AND gate



An "H" signal appears at output A only when an "H" signal is applied to all the inputs simultaneously. (Conjunction AND gate)

E_1	E_2	A
L	L	L
L	H	L
H	L	L
H	H	H

The OR gate



An "H" signal appears at the output when at least one input has an "H" applied to it. (Disjunction)

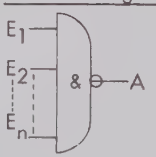
E_1	E_2	A
L	L	L
L	H	H
H	L	H
H	H	H

The NOT gate

The input signal always appears inverted at the output (Inverter)

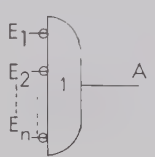
E	A
H	L
L	H

The NAND gate



An L signal appears at the output when an "H" signal is fed in at all inputs

E_1	E_2	A
L	L	H
L	H	H
H	L	H
H	H	L

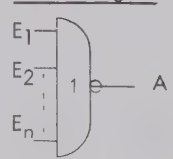


Alternative symbol
De Morgan's rule states the alternative symbol is true whereby:

$A = E_1 \wedge E_2 \wedge \ldots E_n$

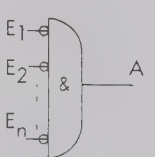
$A = \bar{E}_1 \vee \bar{E}_2 \vee \ldots \bar{E}_n$

The NOR gate



An L signal appears at the output, when at least one input has an "H" applied

E_1	E_2	A
L	L	H
L	H	L
H	L	L
H	H	L



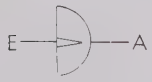
Alternative form
According to De Morgan's rule:

$A = E_1 \vee E_2 \vee \ldots E_n$

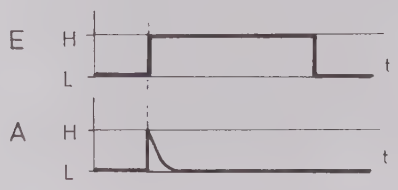
$A = \bar{E}_1 \wedge \bar{E}_2 \wedge \ldots \bar{E}_n$

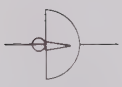
6. PRELIMINARY REMARKS TO SERVICE MANUAL

Differentiators



Symbol for circuits which convert a L-H transition into a L-H-L needle pulse





Symbol for circuits which convert a H-L transition into a H-L-H needle pulse

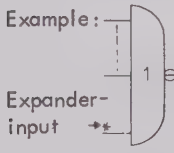
Wired AND

The symbol "wired AND" signifies that two or more circuits are wired in such a way that it simulates an AND logic without actually using an AND logic element

NOR Gate with power fan out

Where the logic element is capable of being loaded, the boundary line at the output side is drawn thick. This signifies that the output from this module is capable of driving several other modules simultaneously. In IC technology this is described as "fan out" capability.

Extending the input circuit by means of an "Expander" input



NOR circuit with four inputs. A further special input permits extending the logic circuit through external circuitry.

6.3.2.3. Bistable circuits with memory behavior

Two different basic types are discussed here: the Flip-Flop (FF) and the monostable (MF)

Flip-Flops

These toggle circuits have two stable states: Depending on the input signal, the flip-flop assumes one of the two states.

If one of the two states is defined as the normal position, then that output which assumes the H status is identified by a block bar.

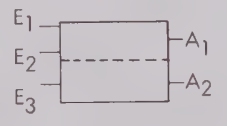
Static input signals (explanation and example)

If the signal at input E_1 changes from L to H, then the FF toggles, independently of the slope of the L-H transition, to the status which is identified by an H status at output A_1. Thus, output A_2 is forced to be in the L status.

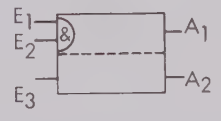
If the signal at input E_1 changes from H to L, then the FF remains in the previously assumed state. Only after the signal changes from L to H at input E_2, does the FF toggle to the second stable status identified by an H status at output A_2, (here taken as the normal position). Output A_1 is then forced to assume L status.
This state is maintained by the FF even though the signal at input E_2 may change from H to L.
Generally it is impermissible, to apply L-H transition signals simultaneously to inputs E_1 and E_2.

E_1	E_2	A_1	A_2	
H↓	L	H	L	
L↓	L	H↓	L	
L	H↑	L↓	H↑	
L	L↓	L	H	
H↓	L	H↓	L↓	
H	H↑			no FF action

If a flip-flop has several inputs without special identifications, then these inputs are disjunctive-coupled (OR gate).
That means:
The flip-flop toggles with a transition from L to H at inputs E_1 or E_2, or at both; the state becomes that identified by an H status at output A_1.

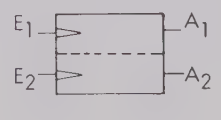


In the following symbol, the inputs E_1 and E_2 are conjunctive-coupled (AND gate).
That means:
The flip-flop first toggles when the two inputs E_1 and E_2 simultaneously assume the H status



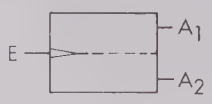
Examples with dynamic signals at the inputs

The symbol represents a FF with two dynamic inputs E_1 and E_2. A L-H transition at input E_1 toggles the Flip-Flop to the state identified by an H appearing at A_1. Similarly a L-H transition at E_2 toggles the Flip-Flop to the state identified by an H appearing at A_2.



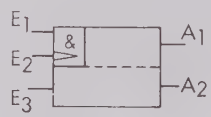
6. PRELIMINARY REMARKS TO SERVICE MANUAL

A symbol ⊳ (or ⊲) shown against the dashed line signifies that the Flip-Flop toggles from one stable state to the other alternately at each L-H (orH-L) transition. Thus an H (or L) appears alternately at A_1 and A_2.



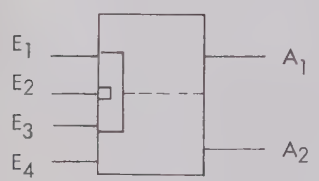
Flip-Flops with preparatory inputs

This Flip-Flop reacts to a L-H transition at the dynamic input E_2 only if simultaneously an H signal is present at input E_1. In this case the Flip-Flop toggles to the state in which an H appears at output A_1. E_3 is a static input.



In the following switching symbol, the dynamic input reacts when the two other inputs have been prepared, i.e. every L-H transition at input E_2 toggles the flip-flop when at the same time an H status exists at input E_1.

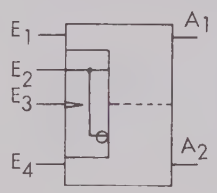
J-K Master Slave Flip-Flop (e.g. SN 7473 from Texas Instruments)



t_n		t_n+1	
E_1	E_3	A_1	A_2
L	L	$\bar{A}_{1n}$	A_{1n}
L	H	L	H
H	L	H	L
H	H	$\bar{A}_{1n}$	A_{1n}

t_n : point of time prior to clock pulse
$t_n + 1$: point of time after clock pulse
E_2 : clock input
E_4 : non-synchronuous reset input (independent from E_2)
"L" at E_4 forces A_1 to "L"

D Type Flip-Flop (edge-triggered) (also as on example of the SN 7474 from Texas Instruments)



Flip-Flop with preparing input E_2 and a higher ordered triggering input E_3

E_1 and E_4 are directly effective at the outputs.

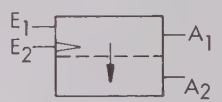
t_n	t_n+1	
E_2	A_1	A_2
L	L	H
H	H	L

Monostable circuits

These also known as one-shot multivibrators. They have only one stable state (normally open) and a quasi-stable state (closed); whereby the arrow is drawn to show which output is in the normally closed state.

Example :
In the following monostable, an L status applied to the static input E_1, or a L-H transition at the dynamic input E_2, toggles the circuit from the normally open status to become the quasi-stable closed status (Hstate at output A_1).

After the retoggle time t_R, whose period is determined by an internal RC network, the monostable toggles back to the normally open status.



6.3.2.4. Delay networks

Delays the transition from L to H

Delays the transition from H to L

The transition from L to H as well as the transition from H to L are delayed, but the delay times are different

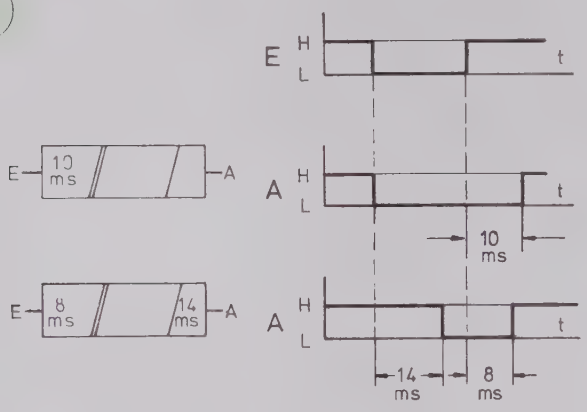
The transition L to H and from H to L are delayed by the same amount

The double slant stroke identifies the input side.

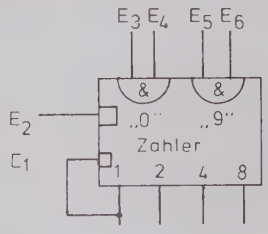
The delay time can be noted on the symbol in units of time, e.g. ms or µs.

6. PRELIMINARY REMARKS TO SERVICE MANUAL

Application examples:



6.3.2.5. BCD decade counter as integrated circuit



Condition for setting to figure 0:
E_3 and E_4 at H status
E_5 or E_6, or both, in L status

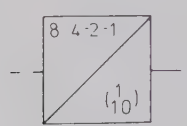
Conditions for setting to figure 9:
E_5 and E_6 at H status
E_3 or E_4, or both, in L status

During counting (pulse input E_2), there must be at least one input in the "L" status at each of the two AND networks.

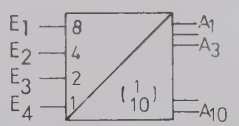
Figure	Outputs			
	1	2	4	8
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

6.3.2.6. Code converter as integrated circuit (IC)

Conversion of the 8-4-2-1 BCD code into the 1 out of 10 code



Simplified (example)



with individual inputs and outputs

6.4. COLOUR CODE

Abbreviations of connection lead colours

bl	blue
bk	barewire
br	brown
fl	transparent
ge	yellow
gn	green
gr	grey
rs	pink
rt	red
Schirm	screened
sw	black
vio	violet
ws	white
wsbl	white/blue
wsbr	white/brown

6.5. HOW TO ORDER REPLACEMENT PARTS

The most important information dealing with replacement parts is found in the component part lists. Component parts with Bv. or WN numbers are to be ordered from the factory.

When ordering replacement parts it is important to state the order number (BN) as well as the equipment number and the position number of the component part, e.g.

BN 691/No. 497601 A/T 202

Order and equipment numbers of the LD-30 Measuring Set may be found on white identification labels in the left handle (front view).

The information dealing with the ordering of replacement printed-circuit boards is obtained from the circuit diagram. It is made up from a boxed number-letter combination, e.g. 691-D. Thus, the complete information required for ordering is, e.g.

BN 691/No. 497601 B/691-D

6.6. EMPLOYED MEASURING EQUIPMENT

The measuring equipment in the Service Instruction Manual for fault finding, checking of specifications and alignment, is listed in this table.

These are recommendations. Equivalent instruments of other manufacturers however may be used.

6. PRELIMINARY REMARKS TO SERVICE MANUAL

Equipment	Type used		In Paragraph
Measuring Set for Group Delay and Attenuation	LD-30	W&G	7.2.1./7.2.2.5./7.2.5./9.2.12.1./ 9.3.6./9.3.13./9.3.14.
Oscilloscope (with 10 · 1 Test Probe)	OS-1 (with TK-4)	W&G	7.2.1./7.2.2./7.2.2.4./7.3.2./9.2.7./ 9.3.5./9.3.6./9.3.8.
Two channel oscilloscope	PM 3240	Philips	9.3.11.
Selective Level Meter	SPM-11	W&G	8.3.
Multimeter	UM	Gossen	7.2.1./7.3.1./9.2.8.
Digital Multimeter	LM 1240	Schlumberger	7.2.2./7.3.2./9.2.5./9.2.9.
Digital Voltmeter	T 2000	H&B	7.2.2.4./8.5./9.1.1./9.2.1./9.2.3./ 9.2.4./9.3.2./9.3.3.2./9.3.7./9.3.12.
Frequency Counter	FZ-4	W&G	7.2.1./7.2.2./8.1./8.7./8.8./9.2.3./ 9.2.4./9.3.9./9.3.12.
Oscilloscope (with 10:1 Test Probe)	OS-2	W&G	7.2.2.4./9.3.13.3
Level Standard	PN 1006	W&G	9.2.9.
Selective Level Meter	SPM-3	W&G	9.3.14.
Selective Level Meter	PMO-8	W&G	8.2.3./8.6./9.3.4.
Selective Level Meter	SPM-6	W&G	9.2.9.
Milliwatt Test Set with Test Probe	EPM 1 with TKS-10 and TKSA-600	W&G	8.2.1./9 2.10.
Distortion Factor Meter	KLM-87	W&G	9.2.7./9.2.8.
Distortion Analyzer	KLA-48	W&G	9.2.6./9.2.7./9.3.9.
Group Delay and Attenuation Standard [1]	LDN-1058	W&G	8.7./8.8./9.3.12.
Logarithmic Attenuator	T 1018	W&G	9.2.9.
Scale Expander	AZD-1	W&G	8.2.3./8.6.

1) The Group Delay and Attenuation Standard LDN-1058 (W&G) is available at our Customer Service Offices.

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

The instructions for fault localization are restricted to the LD-30 Main Frame without ancillary devices.

Information dealing with the fitting, testing and alignment of the various ancillary devices is given in Section 5.3. of the Description and Operating Manual.

A tabulated testing procedure is given for checking the performance of the Generator and Receiver of the Group Delay and Attenuation Measuring Set LD-30. Thus, it is easy to verify the correct functioning of all operating controls, indicators and connectors of the equipment. It is not necessary to open the Set during this checking procedure. Additionally, the tables contain information for localizing a fault in a particular subassembly, which may have become predominantly suspicious after the systematic fault-tracing has been accomplished. The fault can then be pin-pointed using the tables and fault-tracing plans. These tables and plans contain signal forms and nominal levels at important test points, switched status of transistors, output voltages of IC's and logic levels of binary-linking circuits.

All of this information serves to localize faults in the equipment, but does not aid in removing tolerance faults. Tolerance faults are defined as transgressing the guaranteed error limits without noticeable impairment of the equipment operation. For elimination of tolerance errors, see Chapter 9, ALIGNMENT INSTRUCTIONS.

To facilitate fault tracing, different views of the LD-30 are illustrated with annotated positions of test points, subassemblies and alignment elements.

For uniform and simple designation of the operating controls in this Service Manual, the identifying numbers used on the front panel of the LD-30 are also used here.

Coordinating the identifying numbers with the abbreviated designations in the circuit diagrams is done easily by using the table located in Section 2. of the Description and Operating Manual LD-30.

When undertaking repair work, the disassembly instructions should be followed.

In addition to the abbreviations given in Chapter 6. Preliminary Remarks to Service Manual, the following are used:

Measuring frequency	=	MF
Reference frequency	=	REF. FREQ.
Upper sweep limit	=	USL
Lower sweep limit	=	LSL

Statements relevant to logic states in the logic plans of Chapter 7. and in the circuit description Chapter 10. are defined as follows:

$0 \cong +5\,V$
$1 \cong 0\,V$

Transistor status is shown by the following symbols:

○ : transistor nonconducting
● : transistor conducting

The Group Delay and Attenuation Measuring Set LD-30 is always operated in the NORMAL mode, unless otherwise noted. If this operating mode is not to be used, then the fault localization tables will be specially annotated.

7.1. DISASSEMBLY FOR FAULT TRACING

7.1.1. Removal of the equipment panels and the tilting chassis

Caution: Disconnect a.c. line plug before opening the Set.

- The bottom, top and side panels are fastened to the back panel of the Measuring Set with clamping screws. Each panel can be removed after the two corresponding clamping screws have been unscrewed. The panel can then be pulled backwards and removed from the chassis.
- The tilting chassis viewed from above, can be placed in an approx. 80° locked position after the two screws located on the outer chassis strip have been unscrewed. All the printed circuit boards (p.c.b.) shown in photographs 7-3, 7-4, 7-7 and 7-8 are easily accessible.

At the end of the maintenance work, the tilting chassis can be easily pulled up and placed in the fixed position for fastening.

7.1.2. Removing the front panel

If it is necessary to reach the back surface of the front panel, then the following procedure must be adopted, after the cover and bottom panels have been removed:

- The upper and lower trim strips should be removed after the three screws have been unscrewed
- This exposes the front panel screws which should be unscrewed and removed
- The front panel is then carefully drawn forwards at connectors Bu 2301 and Bu 201. The front panel may be moved away by about 10 cm without damaging the connecting cables.

All alignment elements are now accessible.

Replacing the front panel is done in reverse sequence.

7.1.3. Removing a control knob

After the cap has been pried off the top of the knob, the screw or nut at the knob center should be loosened. The knob can then be pulled off the shaft. If the clamping collet does not release itself, then a light tap against the loosened nut or screw should release the knob.

7.1.4. Removing the front cover panel

The front cover panel is fastened to the front panel. For disassembly, the control knobs are removed according to para. 7.1.3. Additionally, five fillister-head screws must be unscrewed, and the front cover panel is then removed from the front of the Set.

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7.2. GENERATOR

In normal operation, the Generator has an alternating and modulated signal over the complete level range of - 50 dBm to + 11 dBm.

Special versions of the LD-30, having been accepted for some Post Office Telephone Lines, accordingly may not be used at + 10 dBm. So as to prevent that level from being transmitted, therefore, level switch [20] is blocked at + 10 dBm on those Measuring Sets.

However, from time to time, during test and alignment work on the Generator and Receiver LD-30, the course level attenuator setting of + 10 dBm is needed. For this reason, it will be necessary to unblock the + 10 dBm position on those special Sets before commencing test and alignment work. After finishing the work, the +10 dBm position should then be reblocked.

The required temporary modification procedure is described in the following.

Disenabling the blocking feature:

- coarse level switch [20] is placed in 0 dBm position
- switch knob is removed according to para. 7.1.3.
- the two visible countersunk screws M 2.5 × 4 mm are loosened until the dial moves freely
- switch knob is replaced (switch position at 0 dBm)
- now, if level switch [20] is rotated clockwise then + 10 dBm also can be set
- test and alignment work can be completed.

Reblocking the position:

- set level switch [20] at 0 dBm
- remove switch knob (see previous instructions)
- rotate disk, with help of wire pin, in counter-clockwise direction until stop is reached
- tighten the two countersunk screws
- replace switch knob (switch position at 0 dBm)

7.2.1. Checking Generator functions

Test instruments required for checking functions.

1 Measuring Set LD-30 or
1 Receiver LDE-3
1 Oscilloscope with 10 : 1 test probe e.g. OS-1 W&G
1 Multimeter e.g. UM Gossen
1 Frequency counter e.g. FZ-4 W&G

Unless otherwise required in the tables, push buttons [28] 3 and 4 are not actuated.

7.2.2. Fault localization at the Generator

7.2.2.1. Measuring configuration for localizing faults at the Generator

For presenting some of the oscilloscope traces given in para. 7.2.2.4., the oscilloscope should be triggered by the output signal at TP 2405.

The sweep rate is adjusted so that the trigger signal (reference time-measuring time) appears as complete,and has

Test of:	Required setting on LD-30 Generator	Necessary measurement agents and their settings		Nominal value and nominal voltage	With defect, probable fault in subassemblies:	Further fault localization · Investigation of following test points in para. 7.2.2.4.
		LD-30 Receiver	Miscellaneous			
Power switch S 101	Connect a.c. power cord Depress S 101			Frequency display and input level readout <– 50 dBm must illuminate	① Power supply equipment fuse S 101	Power supply voltages Para 7.2.2.3.
Level "fine" Potentiometer [5]	Potentiometer [5] at full clockwise stop, MF and VF at 1 kHz	Depress button [31] 5 Switch [33] in 0 dBm position	Connect Bu 2301 to Bu 201	Input level readout < – 50 dBm does not illuminate Meter reading > + 1 dBm	㉓ Modulator and final amplifier	5)
Level "coarse" Switch [20]	Potentiometer [5] in 0 dBm position. Switch [20] in + 10 dBm position. MF and REF. FREQ. at 1 kHz Level varied with switch [20] in 5 dB steps from + 10 dBm to - 45 dBm	Switch [33] in position 0 dBm, –20 dBm and – 40 dBm corresponding to meter scale ranges. Depress push button [31] 5	As above	The reading on meter [10] change in 5 dB jumps	㉓ Modulator and final amplifier	2) 3)
TEST push button [6]	Frequency as above, level at 0 dBm	Reading of attenuation with push button [31] 4, meter scale range ± 5 dB with switch [23]. Reading of group delay distortion with push button [31] 3 meter scale range ± 5 ms with switch [11]	As above	Reading fluctuates by approx. 1 dB on meter [10] Approx. 1 ms	㉔ Modulation frequency generator	TP 2405 14) 23)

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

MEAS. FREQUENCY setting Potentiometer [4]	Depress push button [28] 1 200 Hz to 4 kHz or push button [28] 2 200 Hz to 20 kHz; change potentiometer [4]	Switch [8] to position SENDER	As above	Frequency display must change continuously from 200 Hz to 4 kHz or from 200 Hz to 20 kHz	(25) CF generator	TP 2509 TP 2511 24) 28)
REFERENCE FREQUENCY preselector [25] push button [27]	Adjust preselector [25] e.g. to 3 kHz Depress push button [27]	Switch [8] to position SENDER	As above	3 kHz should be readout at frequency display [9] With deviations of up to 150 Hz, reset with potentiometer [26]	(25) CF generator	28)
UPPER SWEEP LIMIT (USL) preselector [1] push button [3]	Adjust preselector [1] e.g. to 10 kHz Depress push button [3]	Switch [8] to position SENDER	As above	10 kHz should be readout at frequency display [9] With deviations of up to 150 Hz, reset with potentiometer [2]	(25) CF generator	TP 2509 28)
LOWER SWEEP LIMIT (LSL) preselector [16] push button [18]	Adjust preselector [16] e.g. to 2 kHz Depress push button [18]	Switch [8] to position SENDER	As above	2 kHz should be readout at frequency display [9] With deviations of up to 150 Hz, reset with potentiometer [17]	(25) CF generator	TP 2509 28)
CAL potentiometer [2], [17], [26]	Depress corresponding push button, e.g. [3] (USL), [17] (LSL), or [27] REF. FREQ.	Switch [8] to position SENDER	As above	Frequency must be capable of being varied at a frequency of e.g. 1 kHz by an overall ± 300 Hz	(25) CF generator	T 2509 T 2511 24) 28)
SWEEP operation, single shot push button [28] 3	Any SWEEP RATE selected with switch [19]; depress push button [28] 3, then depress push button [3] (USL), and immediately release			At frequency display [9], the relevant frequency, which has been selected at the preselector switch, must appear and remain locked, independant of the settings of push buttons [3], [18] and [27]	(25) CF generator	Logic diagram 4 Voltage diagram 2
	Any SWEEP RATE selected with switch [19]; depress push button [28] 3, then momentarily depress push button [18] (LSL) and immediately release					Logic diagram 2 Voltage diagram 2
	Any SWEEP RATE selected with switch [19]; depress push button [28] 3, then momentarily depress push button [27], REF. FREQ. and immediately release					Voltage diagram 2
START push button [15]	Any SWEEP RATE selected with switch [19]; depress push button [28] 3, then momentarily depress push button [18] and START operation with push button [15]			Frequency changes from LSL→ to USL, at the selected SWEEP RATE	(25) CF generator	Logic diagram 3
SWEEP operation, periodic push button [28] 4	Any SWEEP RATE selected with switch [19]; depress push button [28] 4			Frequency repeatedly sweeps through the adjusted LSL→USL →LSL sequence	(25) CF generator	Logic diagram 5
X-Y Recorder output X-SEND Bu [35]	With depressed push button [28] 2, potentiometer [4] can change frequency continuously from 200 Hz to 20 kHz		Measure d.c. voltage with voltmeter having $Z_{in} \geq 100\,k\Omega$ at connector [35] X-SEND	D.C. voltage must increase proportional to frequency, approx. 0 to + 5 V ≙ 0 to 20 kHz	(25) CF generator	24) Logic diagram 1
GENERATOR OFF	Mode selection switch [22] in position SEND OFF	Measurement range switch [33] in position - 40 dBm; push button [31] 5 depressed	Bu 2301 connected with Bu 201	No level may be indicated Blocking attenuation > 80 dBm	(6) Speech facility (22) Decade switch	S 604/III/b S 2205
	Mode selection switch [22] in position NORMAL, push button [21] depressed					
MOD. OFF	Mode selection switch [22] in position MOD. OFF		Oscilloscope connected to Bu 2301	A signal must appear on the CRO screen, according to point 7.2.2.4. 1)		1)
REMOD (Remodulation)	Place mode selection switch [22] in position REMOD; switch [20] and potentiometer [5] in position 0 dBm	Connect Bu 201 to Bu 2301 of the additional set LD-30	LD 30 additional; connect Bu 2301 to Bu 201 of the additional set	The second LD-30 measures the sent level and provides readings	(25) CF generator (6) Speech facility (2) Input amplifier	S 604 III/a

The frequency counter, in most cases, can only be repaired by the manufacturer. A defective display unit can be changed by the customer. The plugged-in display component is easily accessible after removal of the front cover panel.

Dial tone frequency filters, push buttons [28] 5, [28] 6				Test is accomplished with the retrofitting of the optional printed circuit card "Dial Tone Blocking Filter", BN 691/12. See Operating Manual, para. 5.3.2.		
Remote control of the level				Test is accomplished with the retrofitting of the optional card "Buffer Store for Remote Control of Level", BN 691/11 in the Receiver. See Operating Manual, para. 5.3.1.		
Remote control of the reference frequency				Test is accomplished with the retrofitting of the optional card Reference Frequency Discriminator", BN 691/11 in the Receiver See Operating Manual, para 5 3 1.		
Remote control of the measuring frequency				Test is accomplished with the retrofitting of the optional card "Remote Control of Measuring Frequency", BN 691/11 in the Generator. See Operating Manual, para. 5.3.1.		
D.C. loop-holding circuit				Test is accomplished with the retrofitting of the optional card "D.C. Loop-holding Circuit" BN 691/14 in the Generator. See Operating Manual, para. 5.3.4.		
Switchable Z_{out}/Z_{in} network				Test is accomplished with the retrofitting of the optional card "Switchable Zout/Zin network card" for both Generator and Receiver See Operating Manual, para. 5 3 6		

a 10 cm trace in the horizontal direction. If the trigger signal is not available, the oscilloscope may be triggered internally.

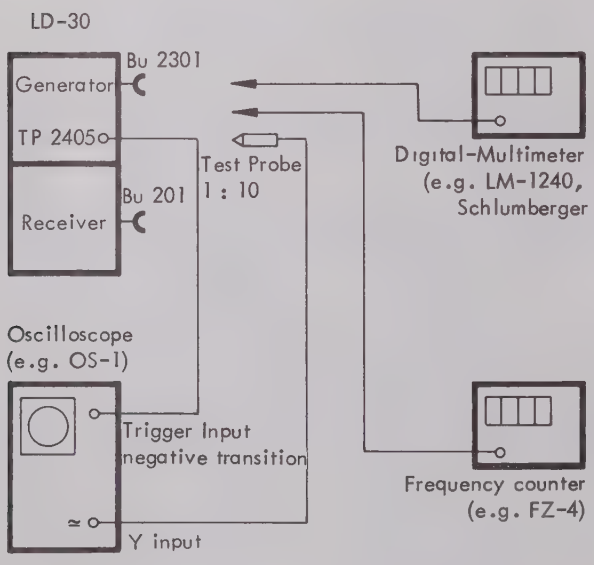


Fig. 7-1

7.2.2.2. Positions of the Generator test points, subassemblies and alignment elements

An LD-30, series A, was used for the photographs in Figs. 7-2 to 7-4.

For simplifying orientation, a relevant section of the housing frame has been photographed and is shown in its normal position (viewed from front panel).

7.2.2.3. Checking the power supply voltages

Before beginning fault localization, with para. 7.2.2.4. at hand for the level, voltage and logic diagrams, it is suggested that the following voltages be checked with a digital voltmeter.

Power supply voltages:

- 12 V ± 0.1 V: point (25) 29 measured to TP 2515 (⊥)
+ 12 V ± 0.1 V: point (25) 28 measured to TP 2515 (⊥)

+ 5 V ± 0.05 V. point (25) 27 measured to TP 2515 (⊥)
+ 6.5 V ± 0.5 V · point (26) b3 measured to TP 2515 (⊥)

Reference voltages:

+ 11.54 V: TP 2505 (+) to TP 2515 (⊥)
+ 7.75 V: TP 2513 (+) to TP 2515 (⊥)
+ 3.083 V to + 3.087 V: TP 2505 (+) to TP 2513 (-)

If there are tolerance errors, see Chapter 9. ALIGNMENT INSTRUCTIONS.

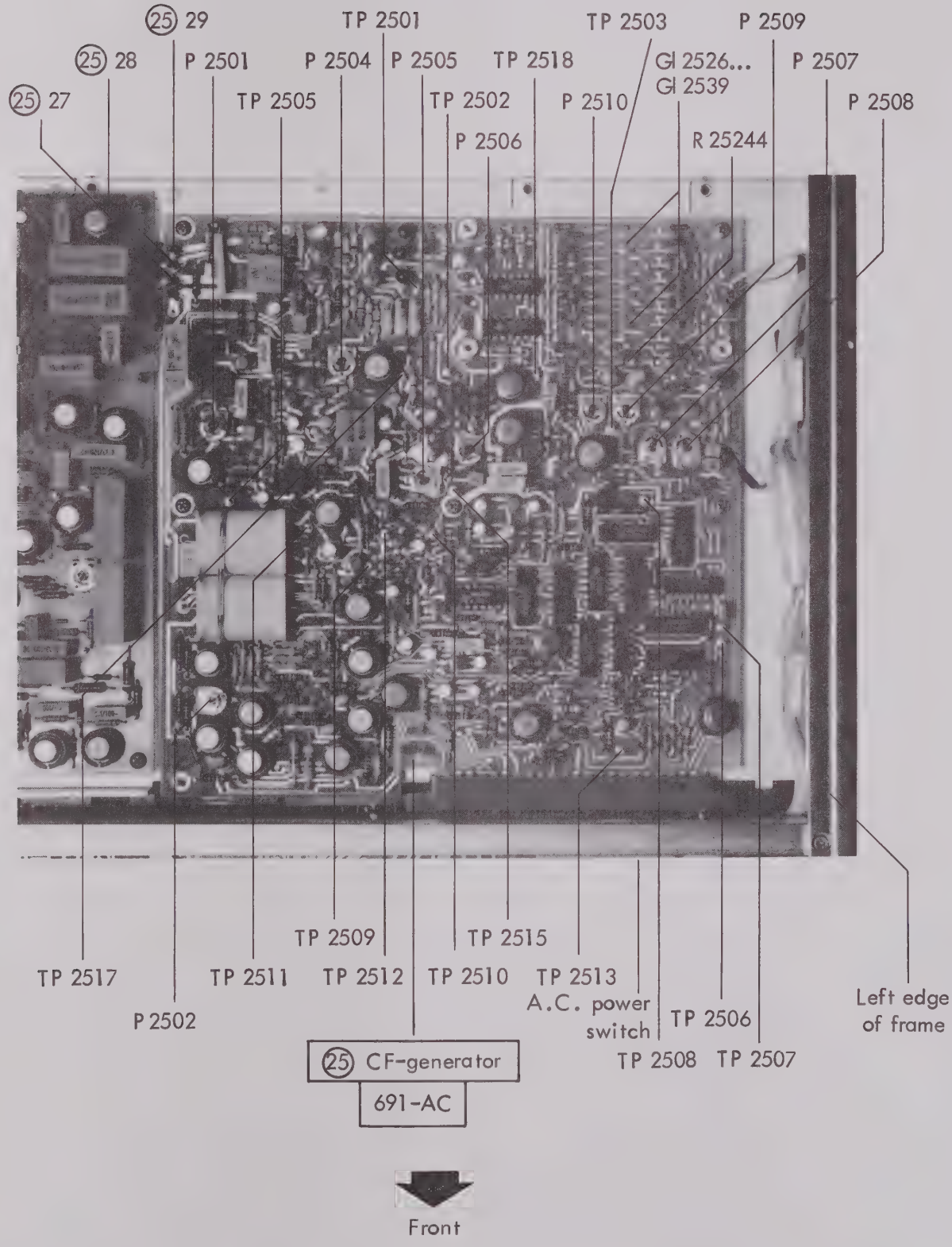


Fig. 7-2 Viewed from below

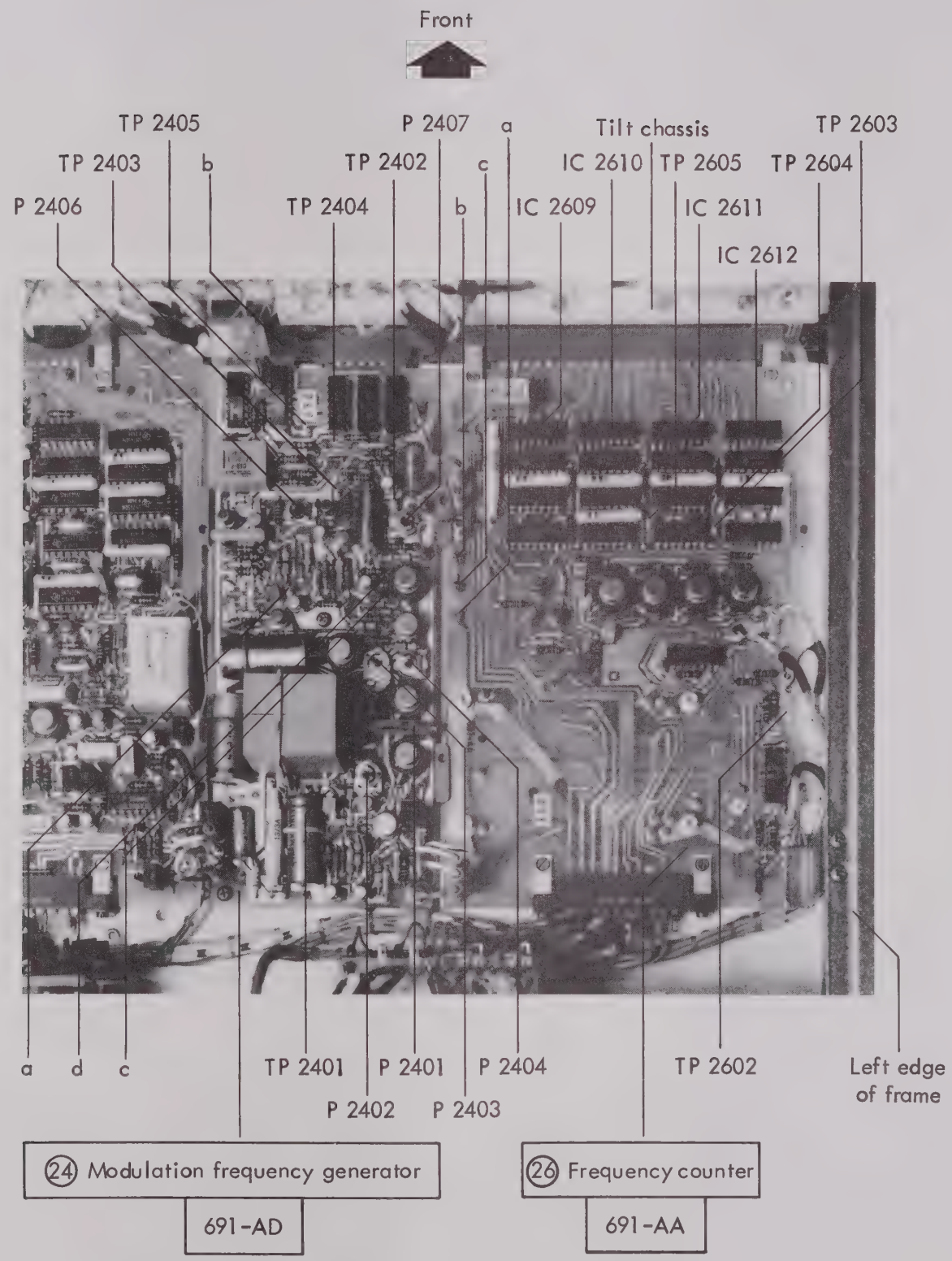


Fig. 7-3 Viewed from above, chassis tilted out

Note: The potentiometers P 2310, P 2311 and P 2312 are shown in Fig. 7-11

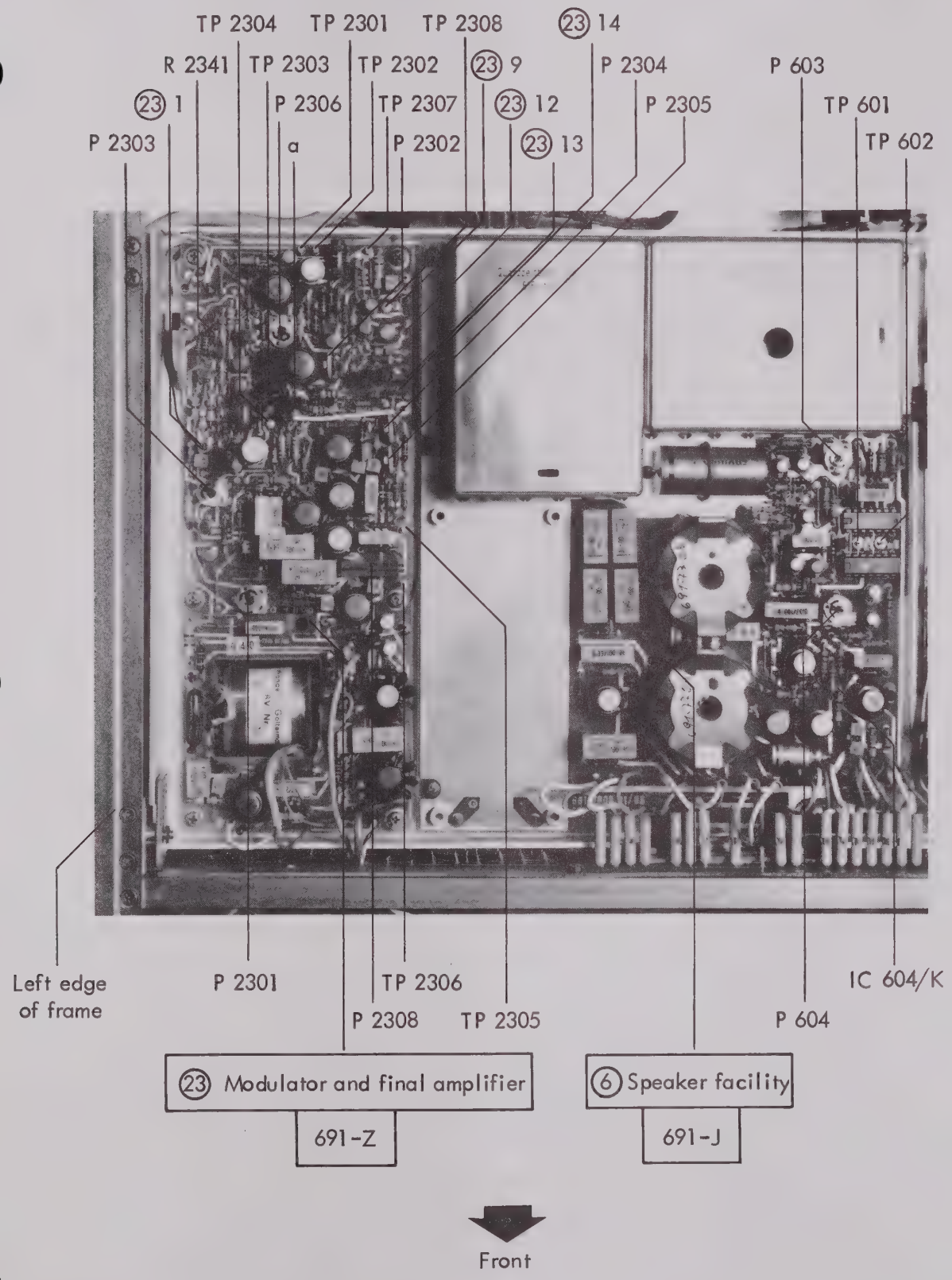
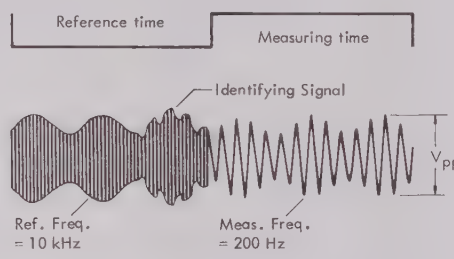
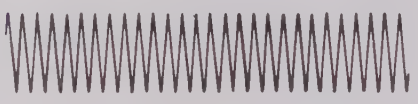
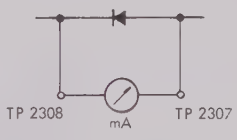
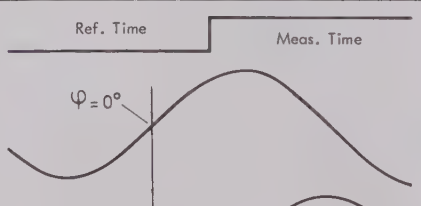
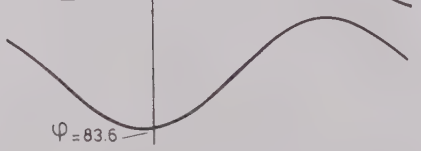


Fig. 7-4 Top view of tilt chassis, left section

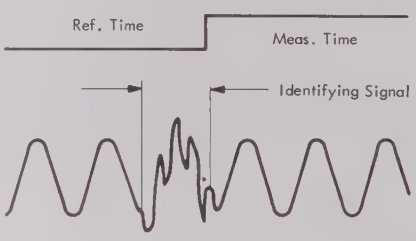
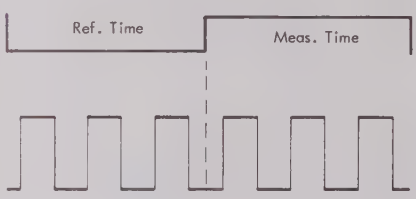
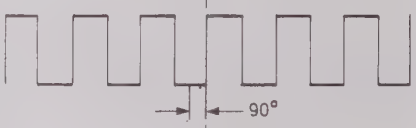
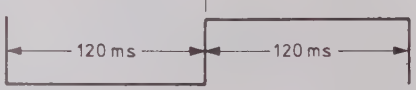
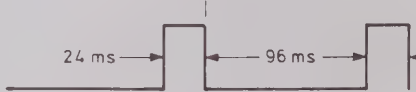
7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7.2.2.4. Tables and diagrams for systematic fault localization

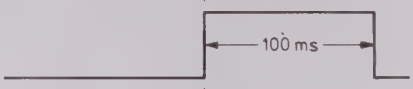
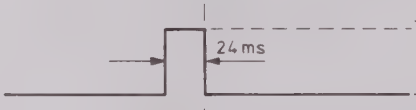
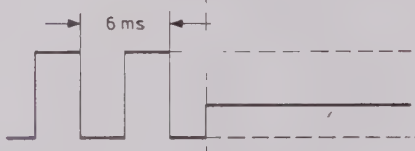
Level diagrams with oscilloscope displays

No.	Test-Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
1)	(23) 1 [691-Z]	V_{pp} = 4.8 V f = 200 Hz to 20 kHz	MF (Carrier)	MOD. OFF	
2)	(23) TP 2306		Trigger Signal Point (24) 12 Send Signal	Normal operation	Output level 0 dBm
3)	(23) TP 2306	 V_{pp} = 11 V	MF	MOD. OFF	Output level 0 dBm
4)	(23) 12 [691-Z]	Signal as on TP 2402 (Test Point No. 9)	41.6 Hz Modulation Frequency with Identifying Signal	Normal operation	
5)	(23) TP 2307-2308	I = 1.0 mA	Modulator current	Normal operation, 0 dBm; output level + 1 dBm	
6)	(24) TP 2401	V_{pp} = 11 V f = 41.66 Hz equivalent to 24.00 ms	Modulation Frequency	Optional	Check frequency with Frequency Counter
7)	(24) TP 2401 (see Fig. 7-3)	 V_{pp} = 11 V	Trigger Signal Point (24) 12 Modulation Frequency		Expansion x 5 at Oscilloscope
8)	(24) Point (H)	 V_{pp} = 4 V	Modulation Frequency	Optional	

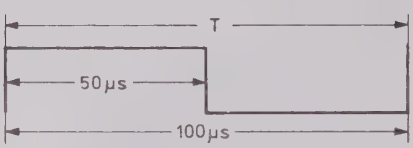
7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test-Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
9)	(24) TP 2402 (see Fig. 7-3)		41.6 Hz Modulation Frequency with Identifying Signal		Printed circuit board 691-AD Bridge c-d closed
10)	(24) Point a 691-AD		Trigger Signal Control Signal		OS-2 Chopper operation
11)	(24) Point b 691-AD		Control Signal		
12)	(24) TP 2403 (see Fig. 7-3)		Identifiying Frequency; t = pulse duration of the 3 ms Monostable	Optional	5 x Expansion at Oscilloscope, 3 ms adjustable with P 2406
13)	(24) Point 12 (B)		4 16 Hz "b" Changeover Signal		
14)	(24) TP 2405		4.16 Hz "a"		
15)	(24) Point (A)				
16)	(24) Point (C)		4 ms Monostable		4 ms adjustable with P 2407
17)	(24) Point (D)				

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
			Trigger Signal		
18)	(24) TP 2404 (see Fig. 7-3)		100 ms gating time		Gating time adjustable with P 2407 (see 4 ms Monostable)
19)	(24) Point (F)		Identifying pulse		
20)	(24) Point (E)		Identifying Signal		
21)	(24) Point (E)		Identifying Signal		5 x expansion at oscilloscope
22)	(24) Point C 691-AD		Identifying Signal		5 x expansion at oscilloscope, bridge c-d open
23)	(24) T 2405/K		Test signal	Test push-button 6 depressed	
24)	Between TP 2511 and TP 2518	Set MF to: / Nominal Value f = 400 Hz — 100 mV f = 10.0 kHz — 2.5 V f = 20.0 kHz — 5.0 V The same voltages are found with LSL, USL, REF. FREQ. set to respective frequencies and push-buttons depressed accordingly	V = (Determining value for MF)	NORMAL	Use Digital Voltmeter 2.5 mV/10 Hz
25)	Between T 2520 and TP 2518	Set REF. FREQ. to / Nominal Value f = 400 Hz — 100 mV f = 10.0 kHz — 2.5 V f = 20.0 kHz — 5.0 V REF. FREQ. push-button depressed and not depressed			

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
26)	Between TP 2517 and TP 2518	Set Frequency to: / Nominal Value LSL: f = 4.00 kHz / 1.0 V USL: f = 8.00 kHz / 2.0 V REF. FREQ. f = 12.00 kHz / 3.0 V MF: f = 16.00 kHz / 4.0 V For the test, the respective push-buttons must be depressed	V = (Determining value for MF)		Use Digital Voltmeter 2.5 mV/10 Hz
27)	㉕ T 2530/K	$V_{\sim}$ = 0 V	Sawtooth voltage	NORMAL	
	㉕ T 2531/K	V_{pp} = 7.6 V MF = 200 Hz to 20 kHz			
28)	㉕ TP 2503 (see Fig. 7-2)	V_{pp} = 7.6 V MF = 200 Hz to 20 kHz	MF (Carrier) at output of triangular generator		
29)	㉕ TP 2502 (see Fig. 7-2)	 V_{pp} = 4 V at MF = 10 kHz (e.g. at MF 1 kHz, T = 1 ms)	Charging direction change-over pulse		The pulse period T corresponds to the set-up MF
30)	Connecting point GI 2541/ GI 2542 R 2544/R 2541 (see Fig. 7-2)	V_{pp} = 4.8 V MF = 200 Hz to 20 kHz	MF (Carrier Oscillation)	MOD. OFF	
31)	㉕ GI 2541/K (see Fig. 7-2)	V_{pp} = 1.4 V	Peak compensation		
32)	㉕ GI 2542/A (see Fig. 7-2)	Signal as at test point 31) but peaks reversed, i.e. pointing upward	Peak compensation		

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
33)	㉕ GI 2532/K (see Fig. 7-2)	V_{pp} approx. 2 V	Sinewave shaper + side	MOD. OFF	Voltage decreases from diode GI 2532 to diode GI 2526
34)	㉕ GI 2526/K (see Fig. 7-2)	V_{pp} approx. 0.1 V	Sinewave shaper + side		
35)	㉕ GI 2533/K and ㉕ GI 2539/K (see Fig. 7-2)	Signals as on Test Points 33) and 34), the pulses point downwards	Sinewave shaper + side		
36)	㉕ TP 2504 (see Fig. 7-2)	V_{pp} = 4.8 V MF = 200 Hz to 20 kHz	MF (Carrier) at output of sinewave shaper		
37)	㉕ TP 2504 (see Fig. 7-2)	120 ms 120 ms 4.16 Hz "b" V_{pp} = 4.8 V REF. FREQ. = 10 kHz MF = 200 Hz	Trigger Signal Carrier changed over between REF. FREQ. and MF	Normal Operation	

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

VOLTAGE LEVEL DIAGRAM 1

Test Point No.	Mode of Operation	Carrier Frequency Change-Over Unit												
		FET-Switch						Output Signal on:						
		T 2519	T 2522	T 2520	T 2523	T 2521	T 2524	IC2517/4.1	IC2517/4.2	IC2518/3.3	T 2518/K			
38)	MF 20 kHz	●	○	○	●	○	●	+5 V	+5 V	0 V	+5 V			
39)	REF FREQ. = 19.9 kHz Push-button 27 depressed	○	●	●	○	○	●	+5 V	0 V	+5 V	+5 V			
40)	Re-transmission REF.FREQ. = 19.9 kHz	○	●	●	○	○	●	+5 V	0 V	+5 V	+5 V			

● = Transistor conducting (Base - 5.2 V, Gate + 2 V at f = 20 kHz)
○ = Transistor nonconducting (Base -6 V : Gate - 5.6 V independent of MF)
Conditions: switch 22 in position MOD. OFF. Push button 28 2 depressed, use digital voltmeter
In the carrier change-over mode there is change-over between REF. FREQ. and MF at a 4.16 Hz rate, i.e. T 2519 and T 2520 are alternately conducting and nonconducting
For locations of test points, see Fig. 7-2

VOLTAGE LEVEL DIAGRAM 2

Test Point No.	Mode of Operation	Control Circuit Switching-Unit				Comparator Output					Schmitt Trigger			
		USL	LSL	REF. FREQ.	MF	USL	LSL	REF. FREQ.	REF. FREQ	MF	USL IC 2504 Point R2515/2516	LSL IC 2505 Point R2517/2518	TP 2511	TP 2509
		T 2503	T 2504	T 2505	T 2506	IC 2506	IC 2507	IC 2509	IC 2508	IC 2510				
41)	Push button 28 2 depressed	●	●	●	○	- 9 V	+11 V	+5.25 V	- 9 V	0 V	+5 V	- 0.6 V	+7.5 V	0 V
42)	Push button 3 (USL) depressed continuously	○	●	●	●	0 V	+11 V	+5 25 V	+11 V	+11 V	- 0.6 V	- 0.6 V	+2.75 V	0 V
43)	Push button 18 (LSL) depressed continuously	●	○	●	●	- 9 V	0 V	+5.25 V	- 9 V	- 9 V	+5 V	+5 V	+7.7 V	0 V
44)	Push button 27 (REF.FREQ.) depressed const.	●	●	○	●	- 9 V	+11 V	+5.25 V	0 V	+11 V	+5 V	- 0.6 V	+5 25 V	0 V
	Push button 28 3 depressed ↓													
45)	Push button 3 (USL) depressed momentarily	○	●	●	●	0 V	+11 V	+5.25 V	+11 V	+11 V	- 0.6 V	- 0 6 V	+2 75 V	0 V
46)	Push button 18 (LSL) depressed momentarily	●	○	●	●	- 9 V	0 V	+5.25 V	- 9 V	- 9 V	+5 V	+5 V	+7.7 V	0 V
47)	Push button 27 (REF.FREQ.) depressed momen.	●	●	○	●	- 9 V	+11 V	+5.25 V	0 V	+11 V	+5 V	- 0.6 V	+5.25 V	0 V
	Single sweep ↓ (⌐)													
48)	Sweep direction from LSL→USL	●	●	●	●	- 9 V	+11 V	+5.25 V	- 9 V	+11 V	+5 V	- 0.6 V	+2.7-7.7 V dependent on instantaneous frequency	- 11 V
49)	Sweep direction from USL→LSL	●	●	●	●	- 9 V	+11 V	+5.25 V	- 9 V	+11 V	+5 V	- 0.6 V		- 11 V

● = Transistor conducting (Base + 0.6 V)
○ = Transistor nonconducting (Base - 5.6 V)
Conditions: LSL = 200 Hz, USL = 20 kHz, REF. FREQ. = 10 kHz, MF = 1 kHz
Use Digital Voltmeter
At 0 V on TP 2509, T 2509 is conducting, at -11 V on TP 2509, T 2509 is nonconducting
Location of test points : see Fig. 7-2

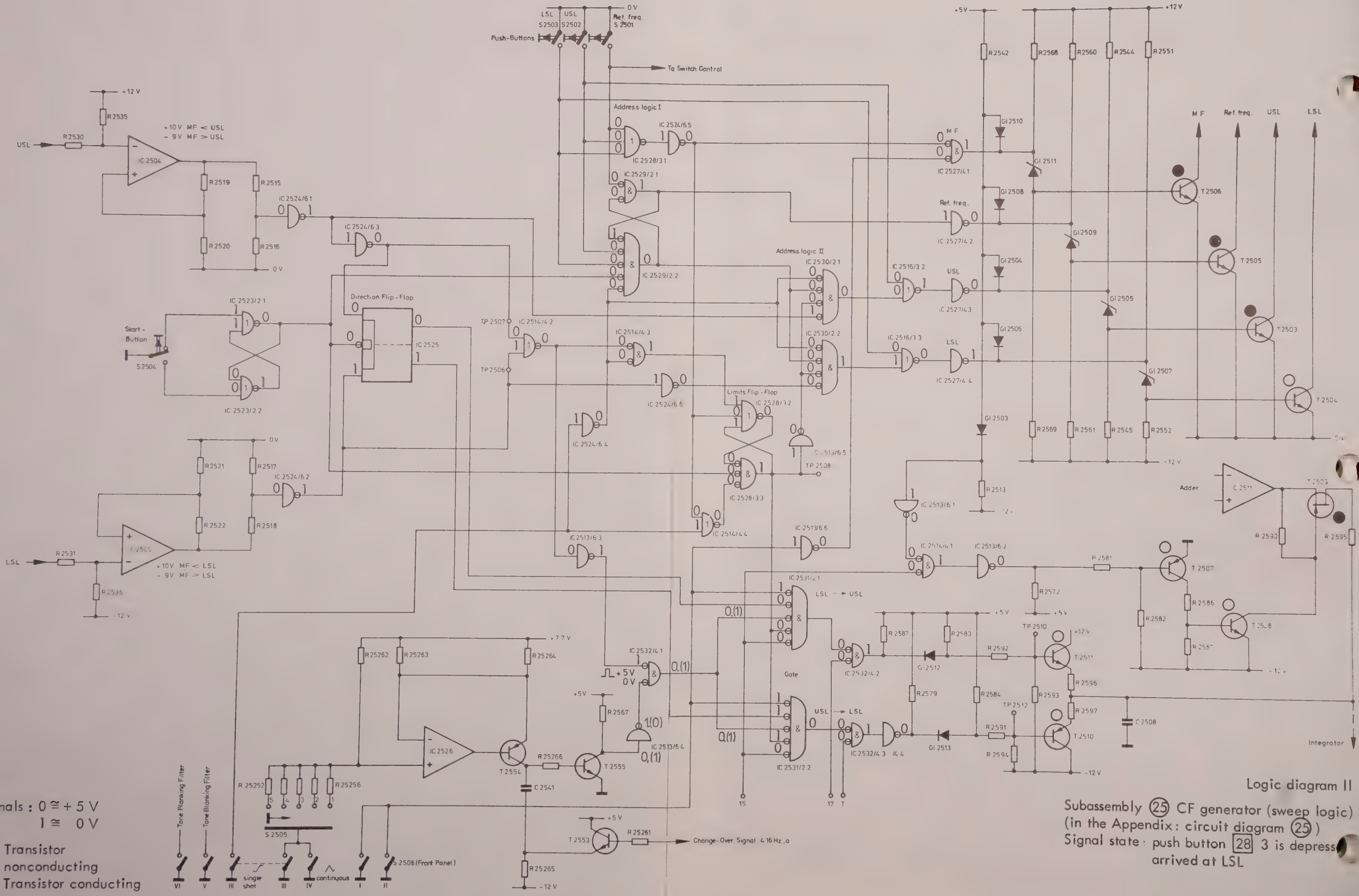
The output signals of the directional flip-flop can be either at 0,1 or (1), (0)

Signals : 0 ≅ + 5 V
1 ≅ 0 V

: Transistor nonconducting
● : Transistor conducting

Logic diagram I

Subassembly (25) CF generator (sweep logic)
(in the Appendix: circuit diagram (25))
Signal state : push button [28] 2 is depressed
switch [22] in position "NORMAL"



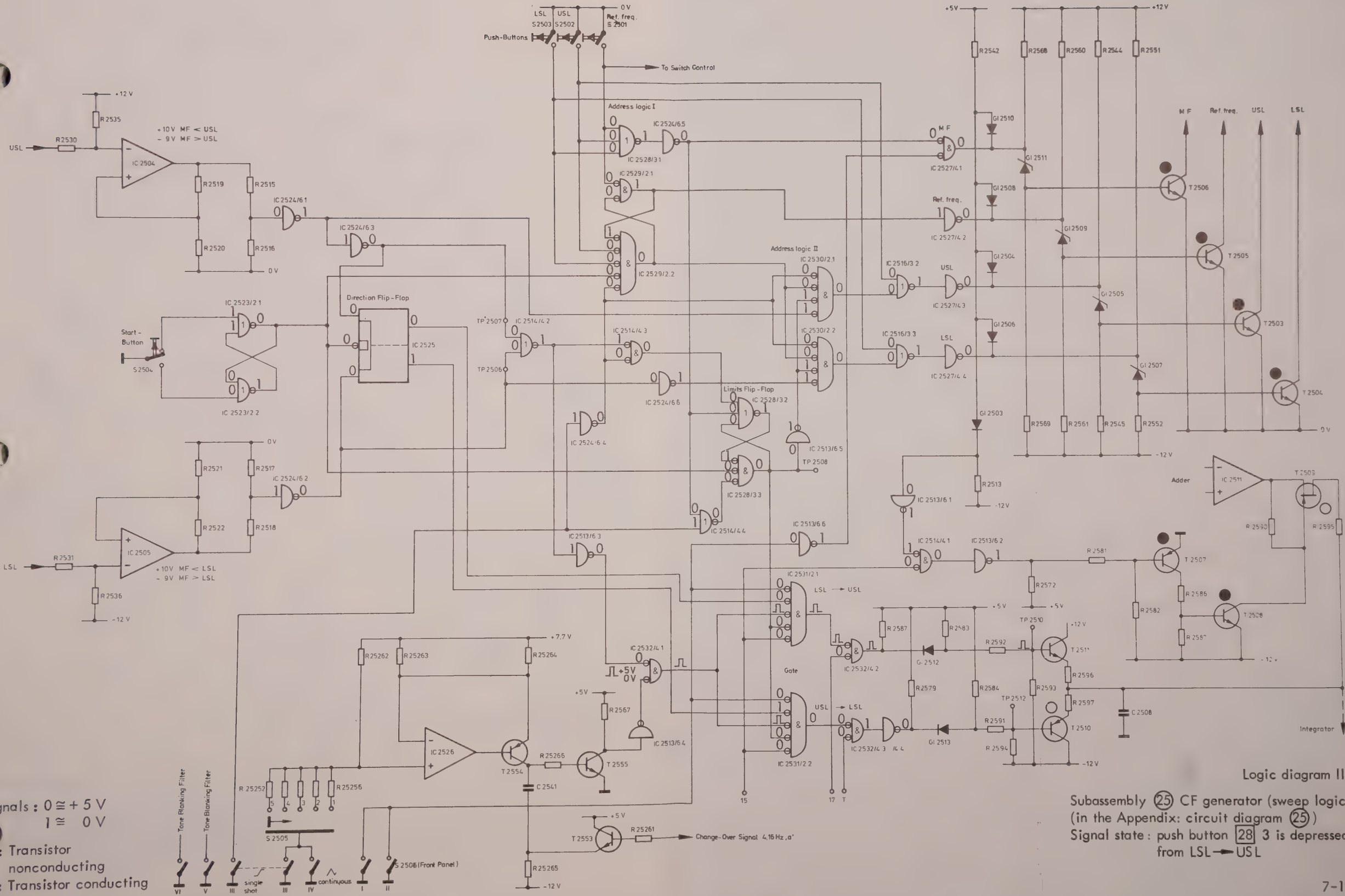
Signals : 0 ≅ + 5 V
1 ≅ 0 V

○ : Transistor nonconducting

● : Transistor conducting

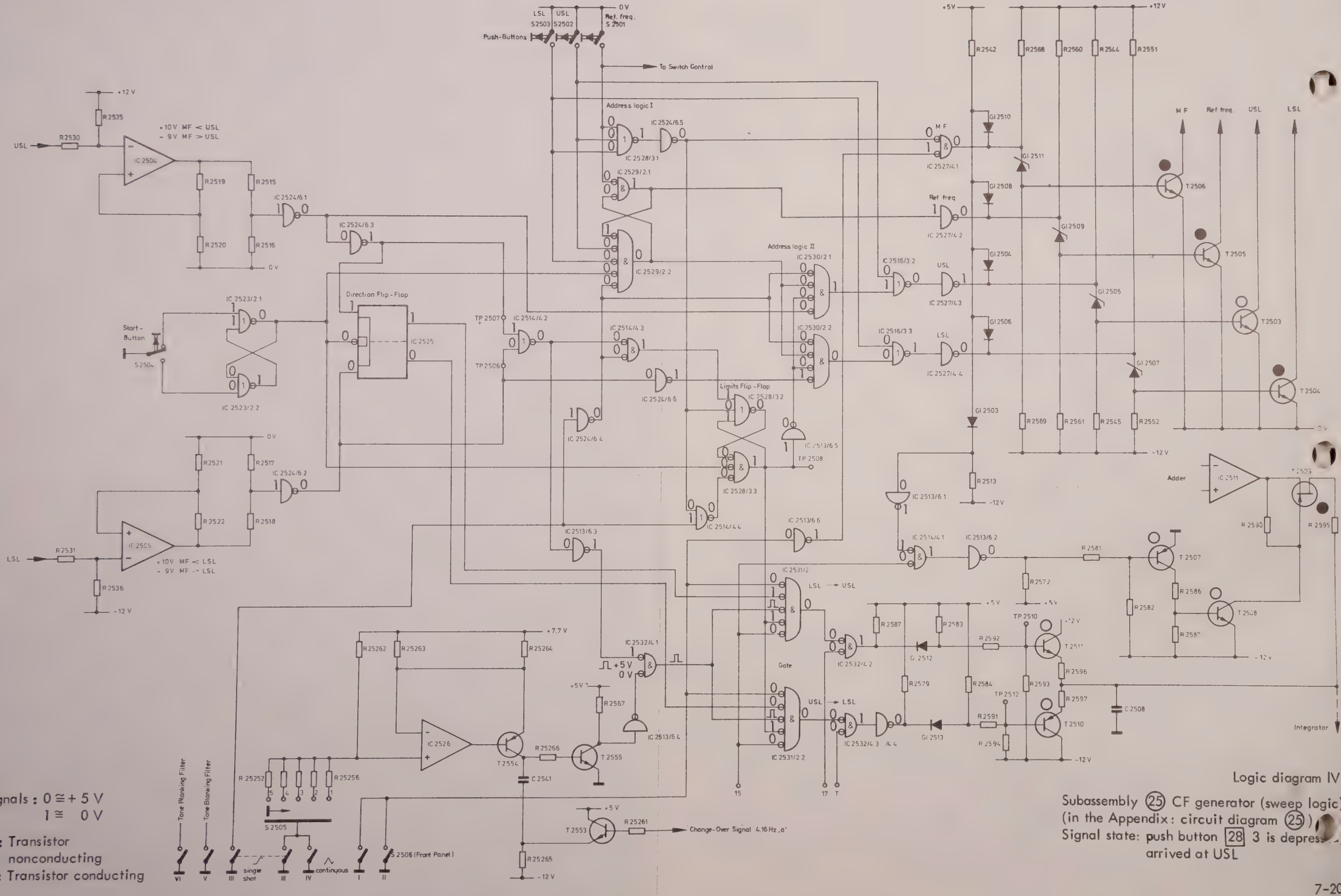
Logic diagram II

Subassembly (25) CF generator (sweep logic)
(in the Appendix : circuit diagram (25))
Signal state : push button [28] 3 is depressed,
arrived at LSL



Logic diagram III

Subassembly (25) CF generator (sweep logic)
(in the Appendix: circuit diagram (25))
Signal state : push button 28 3 is depressed,
from LSL → USL

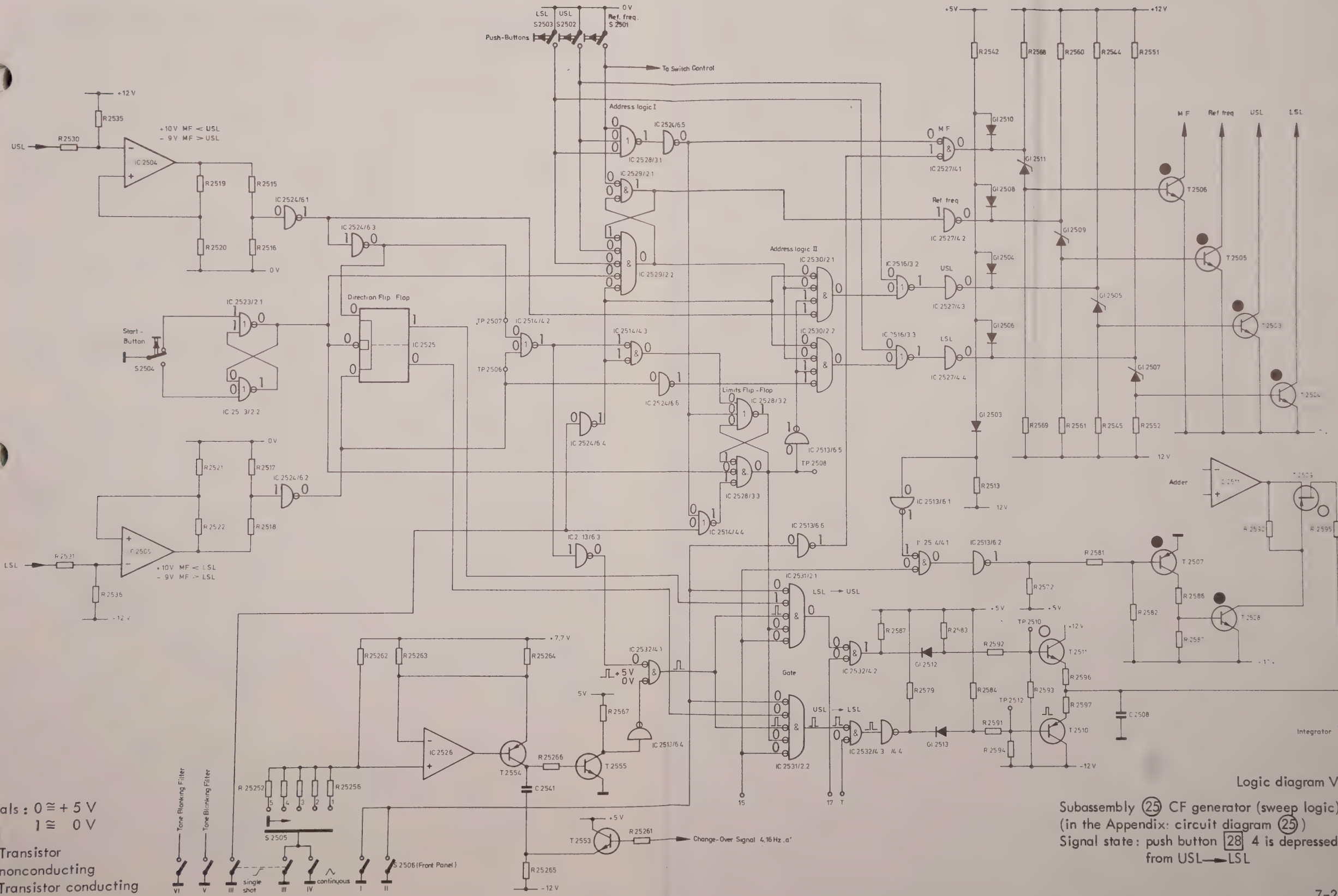


Signals : 0 ≅ + 5 V
1 ≅ 0 V

○ : Transistor nonconducting
● : Transistor conducting

Logic diagram IV

Subassembly (25) CF generator (sweep logic)
(in the Appendix : circuit diagram (25))
Signal state: push button [28] 3 is depressed, arrived at USL



Signals : 0 ≅ + 5 V
1 ≅ 0 V

○ : Transistor nonconducting

● : Transistor conducting

Logic diagram V

Subassembly (25) CF generator (sweep logic)
(in the Appendix: circuit diagram (25))
Signal state : push button [28] 4 is depressed, from USL → LSL

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7.2.2.5. Test with operating mode "remodulation"

Necessary measuring configuration :

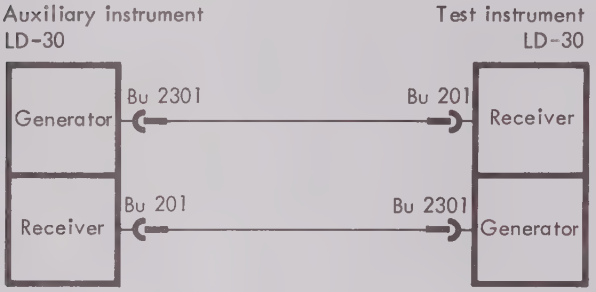


Fig. 7-5

Settings on LD-30 test instrument

- Switch [22] in position "remodulation"
- output level : 0 dBm
- reference frequency : 1.8 kHz
- push button [31] 5 pressed

Settings on LD-30 auxiliary instrument

- reference frequency : 0.4 kHz
  test frequency : 3 kHz
- output level : 0 dBm
- switch [33] set according to send level
- push button [31] 5 pressed
- switch [8] in position RECEIVER

The auxiliary instrument has a receive level 0 dBm ± 0.8 dB.

The frequency readout of the reference frequency 1.8 kHz, remains constant with pressed and unpressed push button [32] .

7.3. RECEIVER

7.3.1. Checking Receiver functions

Test equipment necessary for functional tests

1 LD-30 Generator
1 Multimeter e.g. UM Gossen

Unless otherwise stated in the following table, the following values are set-in at the LD-30 Generator :

- reference frequency : 1.8 kHz
- measuring frequency : 3.0 kHz
- send level : 0 dBm

Switch [22] in position "NORMAL"

Switch [8] in position RECEIVER

Test of :	Required setting on LD 30 Receiver	Necessary measurement agents and their tt ngs		Nominal value and nominal voltage	With defect, probable fault in subassemblies :	Further fault localization : Investigation of following test points in para. 7.3.2.4.
		LD-30 Generator	Miscellanious			
A C line switch (S 101)	Connect power line cord Press S 101			Frequency display must illuminate, level < - 50 dBm must illuminate	(1) Power supply fuse Si 101	Power supply voltage (para. 7.2.2.3.)
Frequency display [9]		Send level, 0 dBm	Bu 2301 connected to Bu 201	Frequency display may not change when switch [8] is changed-over from SENDER to RECEIVER.	(26) Frequency counter (5) Frequency evaluation	
DEC. POINT Push button [7]	Press push button [7]	Send level, 0 dBm MF, 3.0 kHz	As above	Frequency display must switch from 10 Hz to 1 Hz resolution, the 10 kHz place is eliminated	(26) Frequency counter	
Level >+ 10 dBm (GI 403)	Any setting	Send level,+11 dBm	As above	GI 403 must illuminate	(4) Evaluation circuit	5)
Level <- 50 dBm (GI 404)	Any setting	Send level,-52 dBm		GI 404 must illuminate	(Level monitor)	
Level Push button [31] 5	Push button [31] 5 pressed Switch [33] in position 0 dBm Change level to correspond with that set-in at Generator	Send level,+10 dBm Change level in 10 dB steps from 0 to - 40 dB	As above	Meter [10] indicates + 10 dBm Meter [10] must always indicate 0 dBm	(3) Meter amplifier	4)
Group delay distortion Push button [31] 3	Press push button [31] 3 Switch [11] in position + 1 ms Switch [11] changed in position from ± 2 ms to ± 10 ms	Send level,0 dBm Push button [6] pressed	As above	Meter [10] must indicate approx. ± 1 ms Reading must become less according to the selected measuring range	(3) Meter amplifier (4) Evaluation circuit	

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

Atten. distor- on ush button 31 4	Press push button 31 4 Switch 23 in position ± 1 dB Switch 23 in positions ± 2 dB to ± 10 dB	Send level, 0 dBm Push button 6 pressed	As above	Meter must indicate approx. + 1 dB Reading must become less according to the selected measuring range	③ Meter amplifier	
Reference sig- nal Push button 32	Push button 31 5 pressed Switch 33 in position 0 dBm Push button 32 pressed Push button 32 released	Send level, 0 dBm	As above	Meter 10 must indicate 0 dBm Frequency display 9 must indicate 1.8 kHz Frequency display jumps to measuring frequency	③ Meter amplifier	24)
FAST/SLOW meter reading Push button 31 6	Push buttons 31 3 and 31 6 pressed Switch 11 in position ± 1 ms Push button 6 pressed/releas. Push button 31 6 released and push button 6 pressed/ released	Send level, 0 dBm		Reading changes slowly to about + 1 ms Reading changes rapidly to about + 1 ms	③ Meter amplifier	
RECORDER output Bu 35 REC. Bu 34	Push button 31 5 pressed Switch 33 adjusted according to send level	With push button 28 2 pressed, potentiometer 4 is rotated to con- tinuously change frequency from 200 Hz to 20 kHz Change send level from + 10 dBm to - 50 dBm	As above With d.c. volt- meter $Z_{in} \geq 100$ kΩ at Bu 35 and Bu 34	Bu 35 REC : D.C. voltage must change from 0 to + 5 V ≙ 0 to 20 kHz Bu 34 : D.C. voltage must change from -2.5 V to +2.5 V ≙ - 50 dBm to + 10 dBm	③ Meter amplifier ⑤ Evaluation circuit	
Recorder calibrate push button 31 1	Push button 31 5 pressed Switch 33 0 dBm Push button 31 1 pressed	Send level, 0 dBm	Generator output connected to Receiver input (back-to-back operation) D.C. voltmeter $Z_{in} \geq 100$ kΩ at Bu 35	D.C. voltage must be 0 V on Bu 34 and Bu 35	③ Meter amplifier ⑤ Evaluation circuit	
Recorder calibrate push button 31 2	Push buttons 31 5 and 31 2 pressed Switch 33 , 0 dBm	Send level, 0 dBm	D.C. voltmeter $Z_{in} \geq 100$ kΩ at Bu 34	D.C. voltage must be + 2.5 V on Bu 34	③ Meter amplifier	
peaker facility				See operating information and Instruction Manual para. 2.7.	⑥ Speaker facility	34) 35)
Z_{out} switch				See switchable Z_{out} network card, under LD-30 Generator	② Input amplifier	

7.3.2. Fault localization at the Receiver

7.3.2.1. Measuring configuration for localizing faults at the Receiver

In order to be able to check the test points with the use of of the plans in para. 7.3.2.4., the following measuring configuration is required :

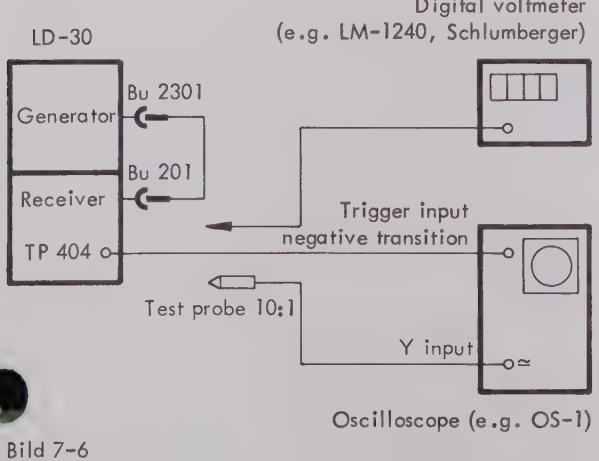


Bild 7-6

When not otherwise stated, the following settings are used :

Generator LD-30 : reference frequency, 1.8 kHz
measuring frequency, 1.8 kHz
send level, 0 dBm
switch 22 in position,"NORMAL"

Oscilloscope : with the signal triggered from LD-30 TP 404 (f = 4.16), adjust sweep rate so that the triggered signal from the LD-30 (reference time - measuring time) appears as a complete image and is displayed over 10 cm, horizontal. (The oscillograms is shown in para. 7.3.2.4. as reduced in size).

7.3.2.2. Positions of the Receiver test points, subassemblies and alignment elements

An LD-30, series A, was used for the photographs in Fig. 7-7 to 7-11.

For simplifying orientation, a relevant section of the housing frame has been photographed and is shown in its normal position (viewed from front panel).

7.3.2.3. Checking the power supply voltages

Before beginning fault localization with para. 7.3.2.4. at hand for the level diagrams, it is suggested that the following voltages be checked with a digital voltmeter :

Power supply voltages :

- 12 V ± 0.1 V : point (4) 16 measured to point (4) 14 ⏚
+ 12 V ± 0.1 V : point (4) 15 measured to point (4) 14 ⏚
+ 5 V ± 0.05 V: point (4) 13 measured to point (4) 14 ⏚

If there are tolerance errors, see Chapter 9. ALIGNMENT INSTRUCTIONS.

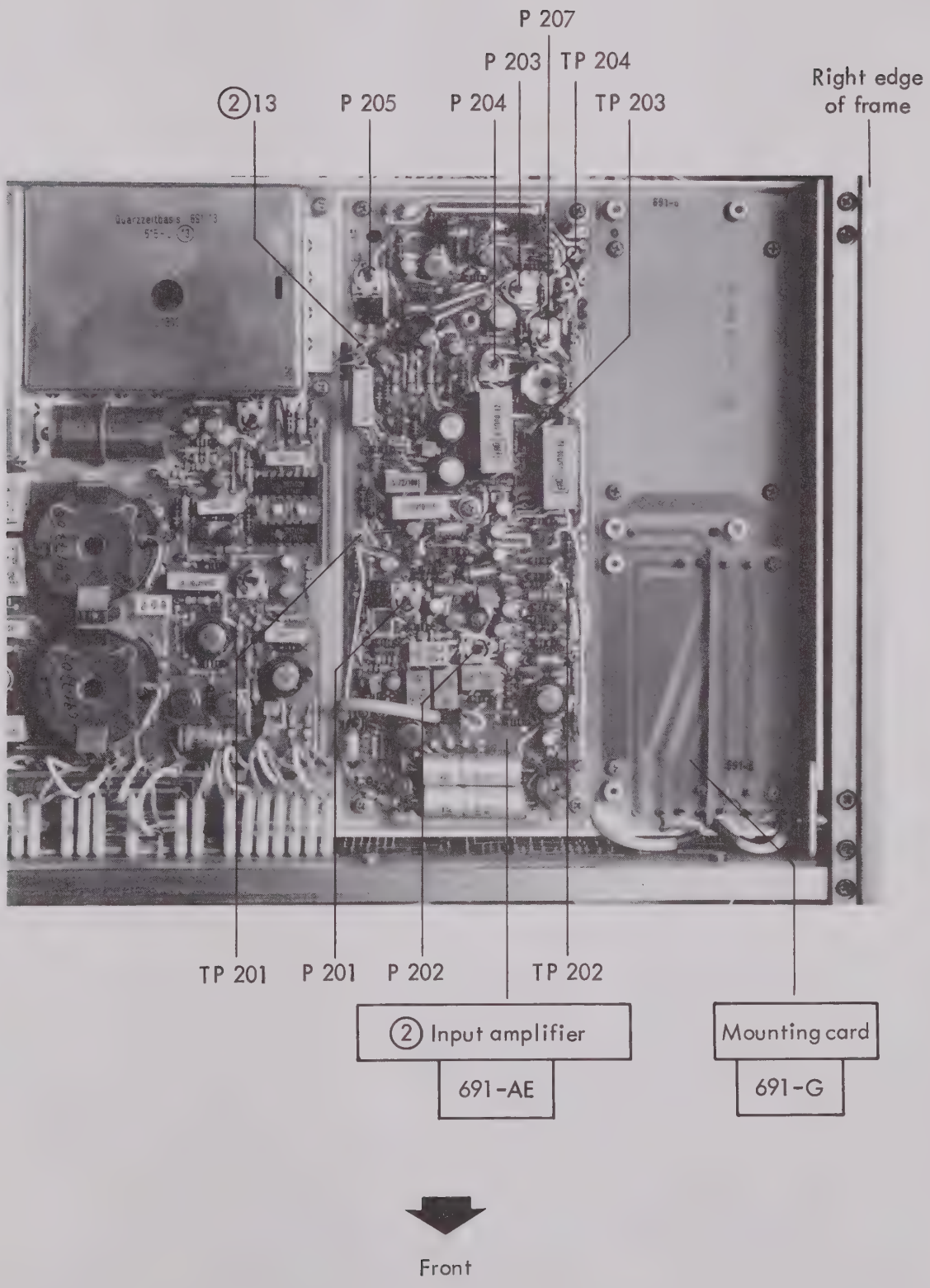
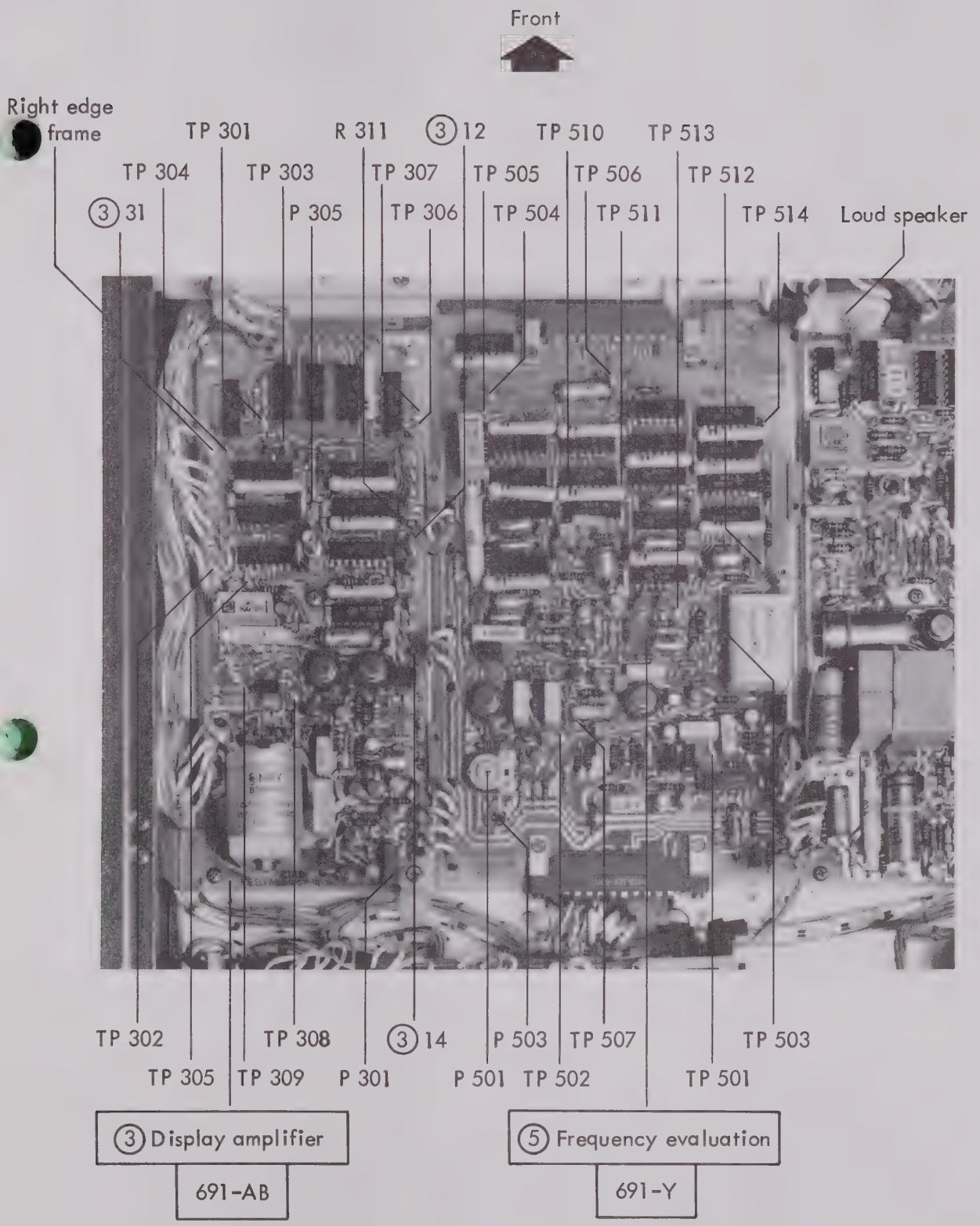


Fig. 7-7 Top view of tilt chassis, right section



Note: The potentiometers P 302, P 303, P 304 and P 502 are shown in Fig. 7-10

Fig. 7-8 Viewed from above, chassis tilted out

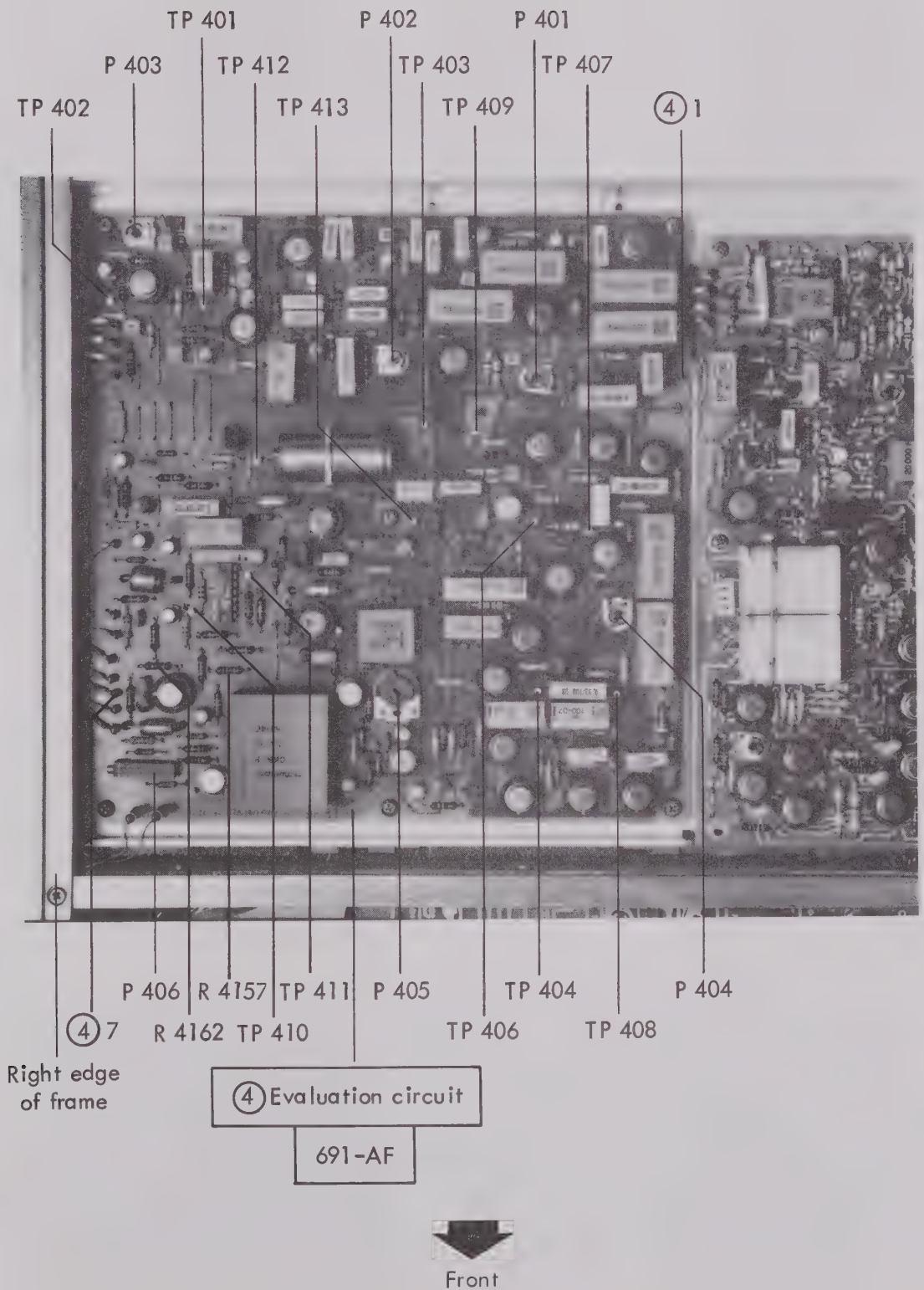


Fig. 7-9 Viewed from below

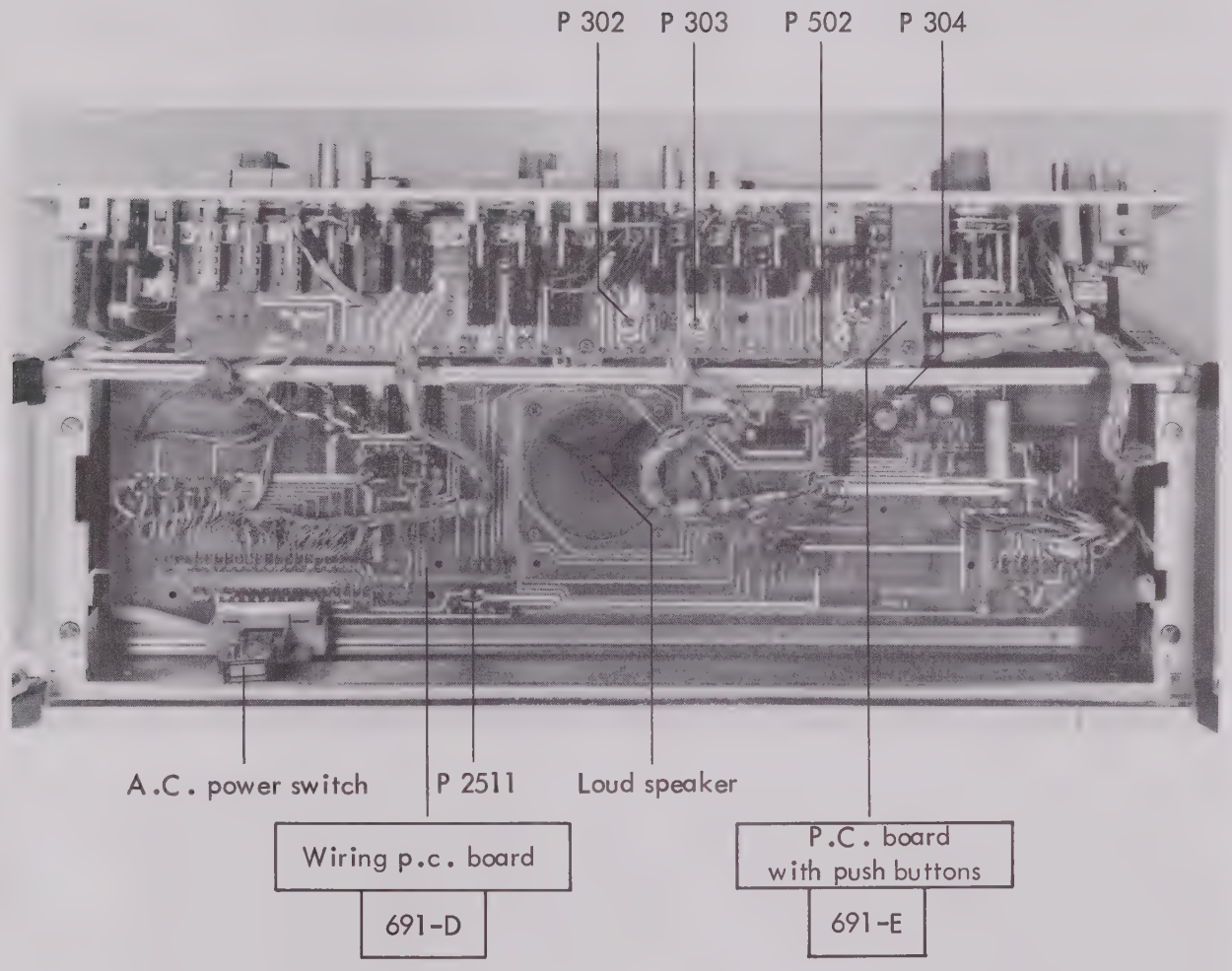


Fig. 7-10 Front view, front panel tilted out upwards

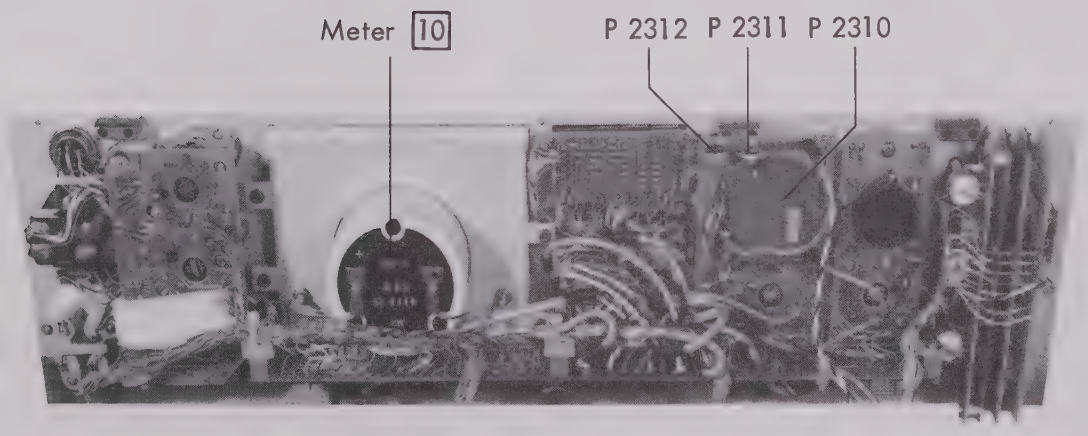


Fig. 7-11 Rear view of front panel

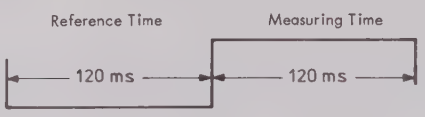
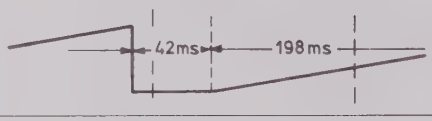
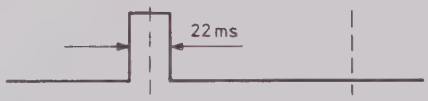
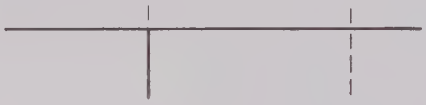
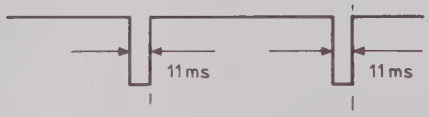
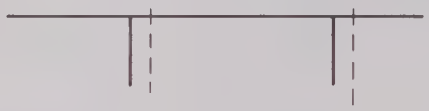
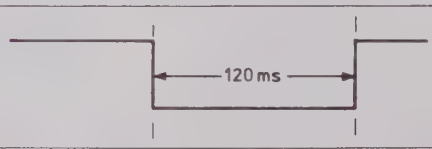
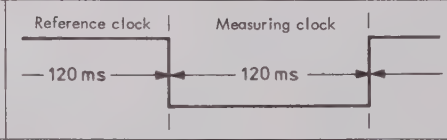
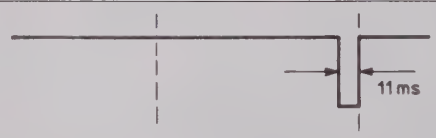
7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

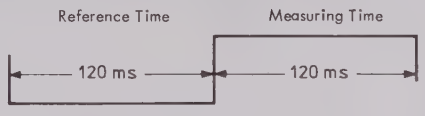
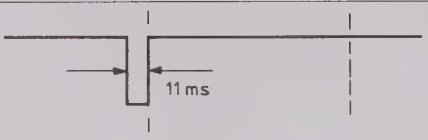
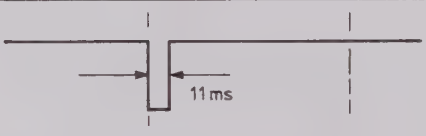
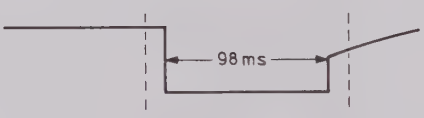
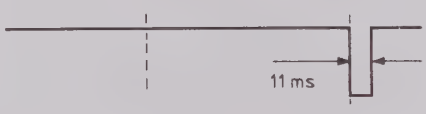
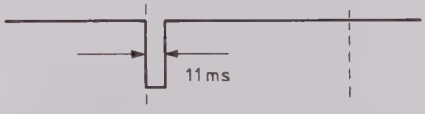
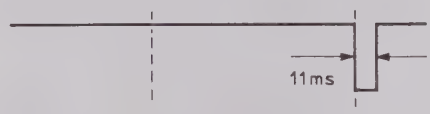
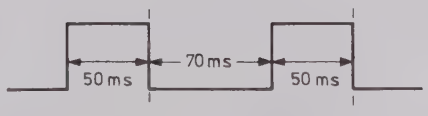
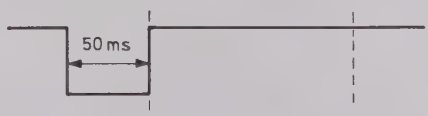
7.3.2.4. Tables and diagrams for systematic fault localization

Level diagrams with oscilloscope displays

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating	Notes
		Reference Time 120 ms — Measuring Time 120 ms — V_{pp} = 5 V, f = 4.16 Hz	Trigger signal 4.16 Hz		derived from TP 2405
1)	② TP 201 TP 202 (see Fig. 7-7)	V_{pp} = 1.5 V, f = 1.8 kHz	Measuring signal	MOD. OFF	Output level on LD-30 : 0 dBm Oscilloscope internally triggered, ~ input
2)	② TP 203 (see Fig. 2-7)	V_{pp} = 0.22 V, f = 41.6 Hz	Split frequency with Identifying signal	NORMAL	Output level on LD-30 : + 10 Trigger signal 41.6 Hz on TP 2401
3)	② 13 691-AE (see Fig. 7-7)	V_{pp} = 0.7 V, f = 41.6 Hz	Split frequency with Identifying signal		
4)	② 13 691-AE (see Fig. 7-7)	+ 1 V at + 10 dBm input level 0 V at 0 dBm input level - 1 V at - 10 dBm input level - 2 V at - 20 dBm input level - 3 V at - 30 dBm input level - 4 V at - 40 dBm input level	DC voltage from logarithmizer		Output level on LD-30 : + 10... - 40 dBm
5)	④ TP 404 (see Fig. 7-9)	- 5.3 V GI 404 level < - 50 dBm must light up + 1.1 V GI 403 level > + 10 dBm must light up	Level too low Level too high		Adjust to nominal level by means of LD-30 output level control (approx. - 52 and + 11 dBm)
6)	④ TP 402 (see Fig. 7-9)	V_{pp} = 5 V, f = 41.6 Hz	Split Frequency		
7)	④ 11 691-AF (see Fig. 7-9)	V_{pp} = 4 V, f = 41.6 Hz	Clock pulses		Pulse width : 270 µs
8)	④ TP 409 (see Fig. 7-9)	V_{pp} = 5 V	Identifying pulses		

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

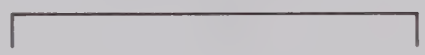
No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
		 V_{pp} = 5 V f = 4.16 Hz	Trigger signal 4.16 Hz		derived from TP 2405
9)	④TP 412 (see Fig. 7-9)	 V_{pp} = 4 V	198-ms-Mono	NORMAL	
10)	④TP 410 (see Fig. 7-9)	 V_{pp} = 5 V	22-ms-pulse stage		
11)	④10 691-AF (see Fig. 7-9)	 V_{pp} = 4 V	Set pulse		Pulse width: 280 µs
12)	④7 691-AF (see Fig. 7-9)	 V_{pp} = 4 V	100-ms-enable		
13)	④9 691-AF (see Fig. 7-9)	 V_{pp} = 5 V	Reset FF 2		Pulse width : 13 µs
14)	④5 691-AF (see Fig. 7-9)		Switching pulses for delay unit 4/14 ms	Switch 11 in position: ± 10 ms add. + 5 ms	
15)	④6 691-AF (see Fig. 7-9)	 V_{pp} = 12 V			
16)	③TP 301 (see Fig. 7-8)	 V_{pp} = 4 V	Measuring/ Reference clock	Optional	
17)	③TP 303 (see Fig. 7-8)	 V_{pp} = 4 V	Charge	NORMAL Push-button 31 3 depressed	

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
		 V_{pp} = 5 V f = 4.16 Hz	Trigger signal 4.16 Hz		derived from TP 2405
18)	③ TP 304 (see Fig. 7-8)	 V_{pp} = 4 V	Discharge	NORMAL Push-button 31 3 depressed	
19)	③ TP 305 (see Fig. 7-8)	 V_{pp} = 4 V	Sample		
20)	③ TP 302 (see Fig. 7-8)	 V_{pp} = 4 V	Clamp		
21)	③ TP 302 (see Fig. 7-8)	 V_{pp} = 5 V	Clamping during attenuation measurement and during reference level measurement	NORMAL Push-button 31 4 depressed	For reference level measurement push-button 32 depressed
22)	③ TP 302 (see Fig. 7-8)	 V_{pp} = 5 V	Clamping during level measurement (Measuring level)	NORMAL Push-button 31 5 depressed	
23)	③ TP 305 (see Fig. 7-8)	 V_{pp} = 4 V	Sampling during level measurement (Measuring level)		
24)	③ TP 305 (see Fig. 7-8)	V_{pp} = 4 V	Sampling during attenuation measurement and during reference level measurement	NORMAL Push-button 31 4 depressed	For reference level measurement push-button 32 depressed
25)	③ IC 304/2.1 Pkt. 4 691-AB (see Fig. 7-8)	 V_{pp} = 4 V	Delay mono-flop 70 ms	Optional	
26)	③ 35 691-AB (see Fig. 7-8)	 V_{pp} = 4 V	Storage Reference Frequency	NORMAL	

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test Point	Nominal Voltage and Nominal Value	Signal Mode	Operating Mode	Notes
		Reference Time 120 ms / Measuring Time 120 ms; V_{pp} = 5 V, f = 4.16 Hz	Trigger signal from 4.16 Hz		derived from TP 2405
27)	③ 12 691-AB (see Fig. 7-8)	50 ms; V_{pp} = 4 V	Synchronisation Measuring Frequency	NORMAL	
28)	③ 12 691-AB (see Fig. 7-8)	50 ms; V_{pp} = 4 V	Synchronisation Reference Frequency	NORMAL Push-Button 32 depressed	
29)	⑤ TP 502 (see Fig. 7-8)	V_{pp} = 6 V, f ~ 1.8 kHz	Measuring signal modulated	NORMAL	Change output level LD-30 from 0 dBm to - 40 dBm, Amplitude must remain constant V_{pp} = 4...5 V, internally triggered, positive edge
30)	⑤ TP 507 (see Fig. 7-8)	V_{pp} = 5 V, f = 1.8 kHz	$f_{Nominal} = f_{Measure}$		internally triggered, positive edge
31)	⑤ TP 501 (see Fig. 7-8)	4 V_{pp} with input level 0 dBm			
32)	⑤ TP 510 (see Fig. 7-8)	2 µs; V_{pp} = 6 V, f = 1.8 kHz	Multivibrator output f_{Actual}		The impulse status changes with the measuring frequency
33)	⑥ 5 691-1	+ 5 V	Supply voltage		With DC Multimeter ($R_i \geq 100$ kΩ/V) against ground (Point 6 or 16)
34)	⑥ 1 691-1	120 ms / 120 ms; V_{pp} = 5 V	4.16 Hz signal	MOD. OFF	In position TALK of operating mode switch 22, no signal is on Pkt, 7 691-1; potentiometer P 601 used for adjustment of needle pulse on center of 20 ms pulse
35)	⑥ 7 691-1	V_{pp} = 4 V	Receiver or Generator signal, resp.		

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

No.	Test Point	Nominal Voltage and Nominal value	Signal Mode	Operating Mode	Notes
		4.16 Hz	Trigger signal		
36)	⑥ TP 602		Needle pulse	MOD. OFF	In position TALK of operating mode switch [22], no signal is on Pkt, 7 [691-1]; potentiometer P 601 used for adjustment of needle pulse on center of 20 ms pulse
37)	T 603/K	230 ms 10 ms	230 ms monostable		
		V_{pp} = 5 V			
38)	⑥ TP 601	20 ms	20 ms monostable		
39)	⑥ 2 [691-1] Point 3 (Input IC 604)	V_{pp} = 5.6 V	AF output	MOD. OFF Potentiometer P 602 in mid position	Connection on Point 10 [691-D] disconnect
40)		V_{pp} = 13 V_{ss}		MOD. OFF Potentiometer P 602 fully clockwise	

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

This section describes methods which permit checking of the important characteristics of the test set. As far as possible commercially available test equipment is used.

If not otherwise specified the tests should be carried out at room temperature (+ 23°C + 3°C) and after a warming up period of 10 minutes.

Checking of the important data is intended to determine whether the indication of a measured value lies within the guaranteed tolerances. This check can be an unrestricted success only if the internal errors of the test configuration used are negligible otherwise the following rule should be used:

If the guaranteed tolerance for the unit to be tested is specified as ±e and if the errors of the test configuration used are ±m, then

an indication outside the tolerance ± (e + m) proves that the guaranteed tolerances are certainly exceeded;

an indication within the limits ±(e-m) proves that the guaranteed tolerances are certainly not exceeded.

The value e is specified for each test. The value m depends on the test equipment used and must therefore be determined from case to case. The test instructions refer to the value of m only if the prescribed test equipment does not permit any variation or if special conditions must be observed.

Alignment of the unit to be tested (in accordance with the references to chapter 9) should be carried out only when the maximum tolerance ± (e + m)is exceeded.

For a systematic check of the data the operations should be carried out in the sequence specified here. If alignment operations are necessary due to excessive errors then these should be carried out before proceeding to the next test.

8.1. TOLERANCES OF THE FREQUENCY INDICATION

The measurement is to be carried out at an ambient temperature in the range +15 to+35°C.

Settings on the LD-30

- Output level: OdBm
- Switch [22] in position "MOD Off"
- Switch [8] in position "GENERATOR"
- Measuring frequency: 10 kHz

Test configuration:

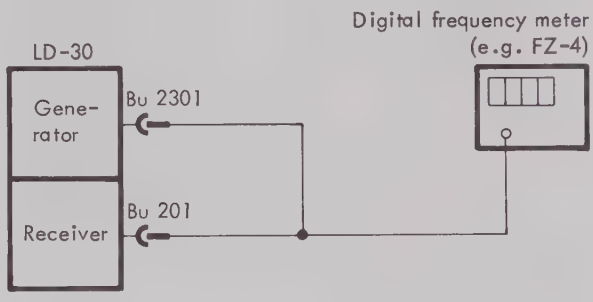


Figure 8-1

Settings on the FZ-4:

- Mode: f/kHz
- Measuring time: 10 s

Read the frequency indication on the FZ-4 and determine the deviation from the indication on the LD-30 with pushbutton [7] depressed.

Tolerance (e) at f=10kHz
±50 Hz ± 1 Digit (≅ 1 Hz)

With crystal time base (BN 691/13) fitted
± 0.1 Hz ± 1 Digit (≅ 1 Hz)

Set switch [8] to position "Receiver" and repeat the test. Additional error ± 1 Hz with respect to the tolerances specified above.

See section 9.2.2. for alignment instructions.

8.2. TOLERANCES OF THE OUTPUT LEVEL, MODULATION FACTOR

The tests in sections 8.2.1. and 8.2.3. detect the important partial errors of the characteristic "Tolerances of the output level".

8.2.1. Tolerances of the output level at 0 dBm

The test is to be carried out at an ambient temperature within the range +15 to + 35°C.

Settings on the LD-30:

- Output level: exactly 0 dBm
- Switch [22] in position "MOD Off"
- Measuring frequency: 1.8 kHz

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

Test configuration :

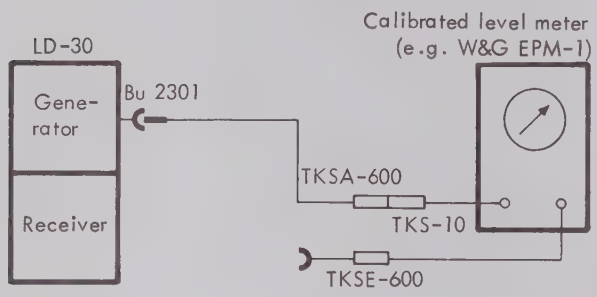


Figure 8-2

Settings on the EPM-1:

- Calibrated by means of TKSE-600, measuring range 0 dBm ± 0.2 dB.

Connect the EPM-1 to the output of the LD-30 and determine the error in the output level.

Tolerance (e): ± 0.12 dB.

See Section 9.2.8. for alignment instructions.

8.2.2. Modulation Factor

- Switch [22] to position "NORMAL"

The modulation results in an increase of the R.M.S. value of the output level by 0.33 dB.

Tolerance (e): 0.30 to 0.365 dB (corresponds to m = 0.4 ± 0.02).

See Section 9.2.7. for alignment instructions.

8.2.3. Tolerances of the Output Attenuator

Test configuration:

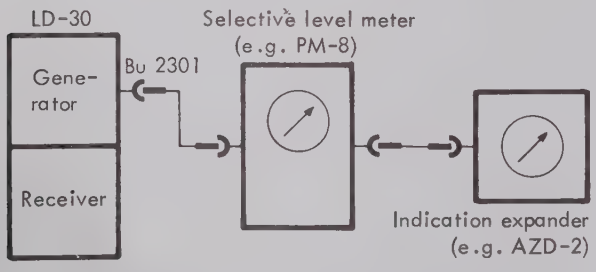


Figure 8-3

Settings on the LD-30

- Output level: 0 dBm
- Measuring frequency: 1.8 kHz
- Switch [22] in position "MOD Off"

Settings on the PM-8:

- Input symmetrical, Z=600 Ohm
- Bandwidth: 300 Hz (eff.)
- Display range of the meter: -6 to+1 dB
- Reception frequency: 1.8 kHz (tune to maximum)
- Level measuring range: 0 dB
- Mode: low distortion

Settings on the AZD-1

- Indication 0 dB

With the above settings adjust the indication of the AZD-1 to exactly 0 dB with the aid of the selective calibration on the PM-8.

- Test all 5 dB stages of the switch [20]. Read off the deviations from the 0 dB indication on the AZD-1.

Tolerance (e) of the output attenuator: ± 0.05 dB.

Test all 1 dB settings of potentiometer [5] starting from 0 dBm (reference setting). Use the 1 dB steps of the AZD-1 for this test.

Tolerance (e) of the fine output attenuator: ± 0.05 dB.

See Sections 9.2.8. and 9.2.9. for alignment instructions.

8.3. HARMONIC RATIO OF THE CARRIER

Test configuration:

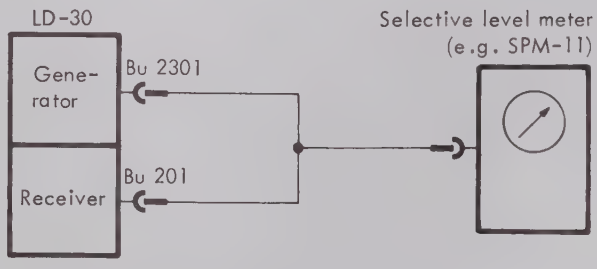


Figure 8-4

The receiver input serves purely as a 600 Ohm termination for the generator output.

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

Settings on the LD-30

- Output level: 0 dBm
- Switch [22] in position "MOD Off"
- Measuring frequency: 1 kHz or 20 kHz

Settings on the SPM-11

Operating mode: low distortion
Level range switch: 0 dB
Selected frequency: 1 kHz or 20 kHz respectively.

Using the SPM-11 measure the harmonic ratio ak_2 and ak_3 with reference to the basic frequency (1 kHz or 20 kHz).

Tolerance (e): ≧ 46 dB.

8.4. CHECK OF THE METER

With the test set switched off and standing on a horizontal surface check the mechanical zero of the meter. If the pointer does not point exactly to "0" carefully adjust it with the screw below the meter.

Switch on the test set and depress the pushbutton [31] 2. The meter [10] must now indicate full scale deflection (scale marking + 10 dBm).

See Section 9.3.3. for alignment instructions.

8.5. ADDITIONAL TEST CONFIGURATION FOR MEASUREMENTS IN SECTIONS 8.6., 8.7 AND 8.8

The test configuration described here can be used additionally for the specified tests. In order to make determination of indication errors more reliable and simple the voltage divider shown in Figure 8-5 is used. It is then unnecessary to read the meter.

Before starting each test the push-button [31] 2 is depressed on the unit being tested and the voltage divider adjusted so that the digital voltmeter indicates + 1000 mV.

Test configuration:

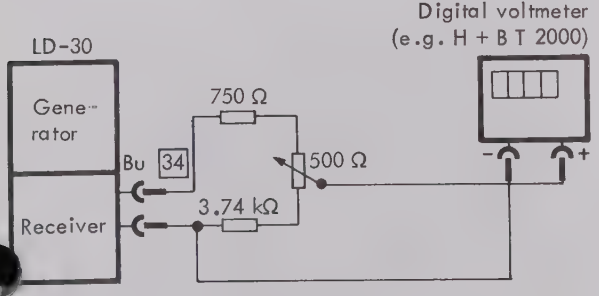


Figure 8-5

This sets up the relationship:

Full scale deflection + 10 dB on meter [10] ≅ 1000 mV.

8.6. TOLERANCES OF THE RECEIVE LEVEL INDICATION

Test configuration:

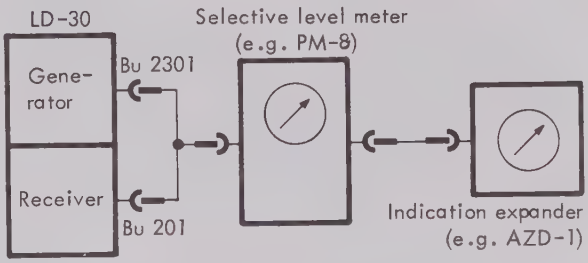


Figure 8-6

The test is to be carried out at an ambient temperature within the range +15 to + 35°C and after a warming up period of at least 1 hour.

Settings on the LD-30:

- Output level: 0 dBm
- Measuring frequency: 1.8 kHz
- Switch [22] in position "MOD Off"

Settings on the PM-8:

- Input symmetrical, R_i = high impedance
- Bandwidth: 300 Hz (eff)
- Display range of the meter: -6 + 1 dB
- Receive frequency: 1.8 kHz (tune to maximum)
- Mode: low distortion
- Level measuring range: 0 dB (unit selectively calibrated)

Note: In order to reduce the internal error (m) of the PM-8 calibration can be carried out as follows:

- In the test configuration shown in Section 8.2.1. , Figure 8-2, measure the transmit level of the LD-30 with the EPM-1 set it exactly to 0 dBm and remove the EPM-1.

- Connect the generator output to the receiver input. In the receiver, determine the deviation from the required value in the measuring range 0 dBm.
  For more accurate reading the test configuration shown in Section 8.5 is recommended. The difference to the required value (=1000 mV) can now be

read from the display of the digital voltmeter.

- Now connect the PM-8 in parallel (test configuration and settings in accordance with Section 8.6) and adjust the output level of the LD-30 until the level meter of the LD-30 (or the digital voltmeter displayed) indicates the error determined in the second paragraph of this note.

- Tune the PM-8 to maximum and adjust the display on the AZD-1 to exactly 0 dB with the aid of the selective calibration.
  After this do not change the calibration of the PM-8/AZD-1.

Setting on the AZD-1:

- Indication 0 dB

All input level values specified in the following table are checked with the receiver PM-8 and set to the required value with the potentiometer [5]

Check the following level measuring ranges of the receiver:

Input level	Level measuring range of receiver	Meter indication	Tolerance (e)	A
+10 dBm	0 dBm	+10 dBm	±0.25 dB	+1000 ± 25 mV
0 dBm	0 dBm - 10 dBm	0 dBm +10 dBm	±0.25 dB	0 ± 25 mV +1000 ± 25 mV
-10 dBm	0 dBm - 10 dBm	-10 dBm 0 dBm	±0.25 dB	-1000 ± 25 mV 0 ± 25 mV
-20 dBm	- 10 dBm - 20 dBm - 30 dBm	-10 dBm 0 dBm +10 dBm	±0.25 dB	-1000 ± 25 mV 0 ± 25 mV +1000 ± 25 mV
-30 dBm	- 30 dBm	0 dBm	±0.60 dB	0 ± 60 mV
-40 dBm	- 40 dBm	0 dBm	±0.60 dB	0 ± 60 mV

Table 8-1

A: The value displayed on the digital voltmeter with the tolerance (e) if the test configuration in Section 8.5 is used.
See Section 9.3.4. for alignment instructions.

8.7. TOLERANCES OF THE ATTENUATION INDICATION

Test configuration:

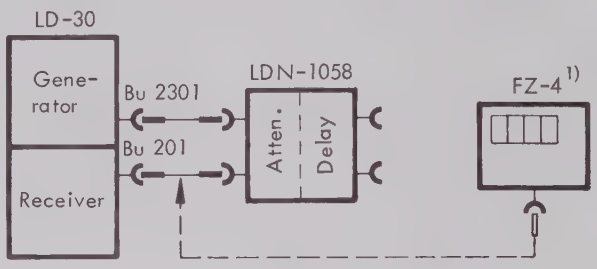


Figure 8-7

1) The digital frequency meter can be omitted if the crystal time base (BN 691/13) is installed in the LD-30.

Settings on the LD-30:

- Output level: + 10 dBm
- Switch [8] in position "GENERATOR"
- Switch [22] in position "NORMAL"
- Setup measuring frequency in accordance with Table 8-2
- Setup reference frequency in accordance with table 8-2
- Pushbutton [31] 4 depressed
- Set the switch [23] to the position corresponding to the attenuation measuring range shown in Table 8-2

Settings on the FZ-4:

- Mode: f/kHz
- Measuring time: 1 s
- Trigger level: continuous "0"

Frequency check:

- Switch [22] in position "MOD Off"
- Check measuring frequency
- Switch [22] to position "NORMAL"
- Depress pushbutton [27]
- Check reference frequency

Note:

The FZ-4 must be connected only for checking the frequency as its load can cause errors in the attenuation indication.

A: The value displayed on the digital voltmeter with tolerance (e) if the test configuration shown in Section 8.5 is used. The specified tolerance (e) also include a value of ± 0.15 dB for the frequency dependent error component and the zero error.

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

These error components can be tested separately if the LDN-1058 is removed from the specified test configuration and if the measuring frequency is varied in the range 0.2 to 20 kHz with a reference frequency of 1.8 kHz

Check the attenuation indication:

Atten. measuring range switch [23]	Set generator to REF. FREQ.	Set generator to MF	Indication	Tol. (e)	A
± 0.5 dB	17.591 kHz	16.330 kHz	+0.5 dB	± 0.16 dB	1000 ± 320 mV
± 1 dB	17.591 kHz	15.212 kHz	+1.0 dB	± 0.17 dB	1000 ± 170 mV
± 2 dB	17.591 kHz	13.315 kHz	+2.0 dB	± 0.19 dB	1000 ± 95 mV
± 5 dB	17.591 kHz	9.375 kHz	+5.0 dB	± 0.25 dB	1000 ± 50 mV
± 10 dB	17.591 kHz	5.790 kHz	+10 dB	± 0.35 dB	1000 ± 35 mV
± 20 dB	17.591 kHz	2.724 kHz	+20 dB	± 0.55 dB	1000 ± 27 mV
± 50 dB	17.591 kHz	0.447 kHz	+50 dB	± 1.15 dB	1000 ± 23 mV

Table 8-2

Tolerances (m) of the attenuation standard LDN-1058:
± 0.4% of the selected attenuation value ± 0.005 dB.

Additional errors if the reference or measuring frequency deviates from specified value:
± 0.07%/1 Hz.

There are no alignment facilities provided for the function "attenuation measurement". The measured values and alignment are combined with those for the level measurement.

8.8 TOLERANCES OF THE GROUP DELAY INDICATION

Test configuration:

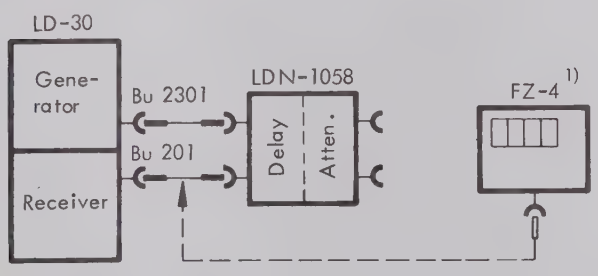


Figure 8-8

1) The digital frequency meter can be omitted if the crystal time base (BN 691/13) is installed in the LD-30.

The test is to be carried out at an ambient temperature within the range + 15 to + 35 °C.

Settings on the LD-30:

- Output level: 0 dBm
- Switch [8] in position "GENERATOR"
- Setup measuring frequency in accordance with Table 8-3
- Setup reference frequency in accordance with Table 8-3
- Switch [22] in position "NORMAL"
- Pushbutton [31] 6 depressed
- Pushbutton [21] 3 depressed
- Set switch [11] in accordance with the group delay measuring range shown in Table 8-3.

Settings on the FZ-4

- Mode: f/kHz
- Measuring time: 1 s
- Trigger level: continuous "0"

Frequency check:

- Switch [22] in position "MOD Off"
- Check measuring frequency
- Switch [22] in position "NORMAL"
- Depress pushbutton [27]
- Check reference frequency

Note:

The FZ-4 may be connected only for frequency checks as its load can cause errors in the group delay indication.

Check the group delay indication:

Delay measuring range switch [11]	Set generator to REF. FREQ.	Set generator to MF	Indication	Tol. (e)	A
± 0.05 ms	2.031 kHz	1.808 kHz	+ 0.05 ms	± 6 µs	1000 ± 120 mV
± 0.1 ms	2.031 kHz	1.674 kHz	+ 0.1 ms	± 7 µs	1000 ± 70 mV
± 0.2 ms	2.031 kHz	1.511 kHz	+ 0.2 ms	± 9 µs	1000 ± 45 mV
± 0.5 ms	2.031 kHz	1.271 kHz	+ 0.5 ms	± 15 µs	1000 ± 30 mV
± 1 ms	2.031 kHz	1.000 kHz	+ 0.9 ms	± 25 µs	900 ± 25 mV
± 2 ms	2.031 kHz	1.000 kHz	+ 0.9 ms	± 45 µs	450 ± 22.5 mV
± 5 ms	2.031 kHz	1.000 kHz	+ 0.9 ms	± 105 µs	180 ± 21 mV
± 10 ms	2.031 kHz	1.000 kHz	+ 0.9 ms	± 205 µs	90 ± 20.5 mV
10 ms add. 5 ms	2.031 kHz	1.000 kHz	- 4.1 ms	± 305 µs	- 410 ± 20 mV

Table 8-3

A: Value displayed on the digital voltmeter with tolerances (e) if the test configuration shown in Section 8.5 is used.

The specified tolerances (e) include a total of ± 5 µs for the zero error and frequency dependent errors (in the range 1 kHz to 20 kHz).

It is possible to test these error components separately if a direct connection is made from the generator to the receiver with a reference frequency of 1.8 kHz.

Tolerances (m) of the delay standard LDN-1058 for all specified delay values: ± 0.5% ± 1 µs.

Additional errors if the reference or measuring frequency deviates from the specified value : ± 0.3%/1 Hz.

See Section 9.3.12.for alignment instructions.

9. ALIGNMENT INSTRUCTIONS

9. ALIGNMENT INSTRUCTIONS

If the test set LD-30 does not operate correctly or if the specified tolerances (e + m) specified in chapter 8 are exceeded when checking the technical data then this chapter gives information concerning the necessary adjustment and alignment measures.

If not otherwise specified the alignment operation should be carried out at room temperature (+ 23°C) and after a warming up period of 10 minutes.

9.1. POWER SUPPLY UNIT

The printed circuit board [691-B] of the power supply unit is fixed to the rear wall of the test set.

9.1.1. Supply Voltages (P 101, P 102, P 103)

The supply voltages are supplied centrally by the power supply unit for the generator and receiver. The voltages can be checked in the generator or receiver at the test points specified in Table 9-1. The measurements are carried out with reference to TP 2515 (⊥) in the generator or point (4) 14 (⊥) in the receiver.

The potentiometers P 101 to 103 are accessible when the swivel chassis on the power supply board is opened.

Required test equipment:
1 Digital voltmeter such as H + B Model T 2000.

Voltage	Test point Generator	Test point Receiver	Alignment potentiometer	Required value
- 12 V	(25) 29	(4) 16	P 103	-12.0 to -12.05 V
+ 12 V	(25) 28	(4) 15	P 102	+12.0 bis +12.05 V
+ 5 V	(25) 27	(4) 13	P 101	+5.0 bis +5.05 V

Table 9-1

9.2. GENERATOR

9.2.1. Reference Voltage for Carrier Frequency Generation (P 2510)

Required test equipment:

Digital voltmeter such as H + B Model 2000.

- Connect digital voltmeter to TP 2513 (-) and TP 2505 (+)
- Adjust potentiometer P 2501 so that the indication is between 3.803 and 3.807 V (preferably 3.805 V)
- The following voltages, which result from the adjustment of the 3.805 V value, should be checked:
  TP 2515 (-) to TP 2513: theoretical value + 7.75 V
  TP 2515 (-) to TP 2505: theoretical value + 11.54 V
  TP 2505 (-) to point (25) 28: V_R 2501 = 0.4 to 0.55 V.

If the value of V_R 2501 is not within the specified range the + 12 V supply should be adjusted with P 102.

9.2.2. Alignment of the Assemblies (24) Modulation Frequency Generation and (25) Carrier Frequency Generation

The following test configuration must be set up for the measurements in Section 9.2.2.:

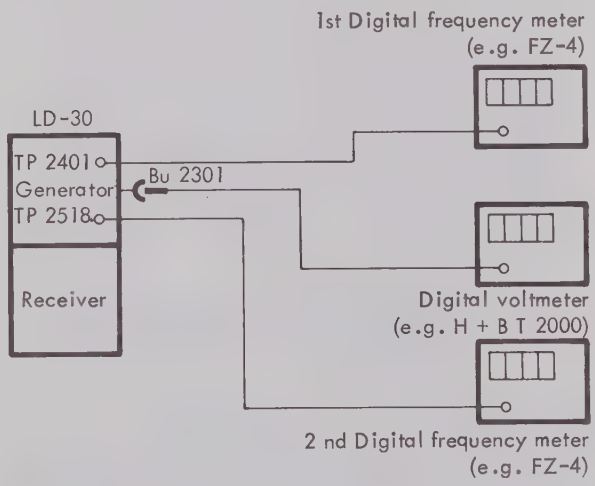


Figure 9-1

Preparation and settings on the LD-30

- Remove identification signal strap c-d on card [691-AD] (24) Modulation Frequency Generation)
- Switch [8] to position "GENERATOR"
- Operating mode switch [22] in position "MOD Off"
- Pushbutton [28] 2 depressed
- LSL: 0.4 kHz
- USL: 6 kHz
- Reference frequency: 10 kHz
- Measuring frequency: approx. 20 kHz

Settings on first digital frequency meter:

9. ALIGNMENT INSTRUCTIONS

- Connect digital frequency meter between TP 2401 and ground (⊥)
- Set to period length measurement (measuring range 10 periods)

Settings on second digital frequency meter:

- Connect digital frequency meter to generator output Bu 2301
- Frequency measurement (measuring time 1 s)

Settings on digital voltmeter:

- Connect digital voltmeter between TP 2518 (+) and TP 2511 (-) Setup so that last readable digit is 1 mV.

9.2.2.1. Modulation Frequency 41.66 Hz and Gate Time "100 ms" for the Internal Frequency Counter Without Crystal Time Base BN 691/13 (P2401, P 2407)

If a crystal time base is fitted it must be removed for this alignment.

- Adjust potentiometer P 2401 so that the first digital frequency meter indicates 24000 ± 20 µs .
- Adjust potentiometer P 2407 (gate time 100 ms) so that the internal frequency indication agrees with the indication on the second digital frequency meter (frequency of the output signal). Pushbutton [7] depressed.

9.2.2.2. Modulation Frequency 41.66 Hz and Gate Time "100 ms" with Crystal Time Base BN 691/13 Installed

If the tolerances of the frequency display are exceeded (see Section 8.1) the crystal time base must be aligned in accordance with the instructions in the description and operating instructions, Section 5.3.3.

9.2.2.3. Frequency/Voltage Linearity of the Carrier Frequency Generation (P 2504, P 2505, P 2506)

Preparation:

- Adjust potentiometer [4] so that exactly 5000 mV are indicated on the digital voltmeter
- Depress pushbutton [28] 3
- Depress pushbutton [18] and adjust potentiometer [17] until the value LSL 100 mV ≅ 400 Hz is displayed on the digital voltmeter
- Depress pushbutton [3] and adjust potentiometer [2] until the value USL 1500 mV ≅ 6000 Hz is displayed on the digital voltmeter
- Depress pushbutton [27] and adjust potentiometer [26] until the value reference frequency 2500 mV ≅ 10000 Hz is indicated on the digital voltmeter.

Alignment operations: see also Figure 9-2

- Depress pushbutton [18] and adjust potentiometer P 2504 so that the output frequency is 400 Hz ± 1 Hz (≅ 100 mV)
- Depress pushbutton [3] and adjust potentiometer P 2505 so that the output frequency is 6000 Hz ± 5 Hz (≅ 1500 mV)
- Depress pushbutton [28] 2 and adjust potentiometer P 2506 so that the output frequency is 20000 Hz ± 20 Hz (≅ 5000 mV)
- Repeat steps 1 to 3 until the specified tolerances are attained
- Depress pushbutton [27] and check that the value 10000 Hz ± 10 Hz (≅ 2500 mV) is displayed
- Replace the identification signal strap c-d.

Deviation of the measuring frequency from the theoretical value

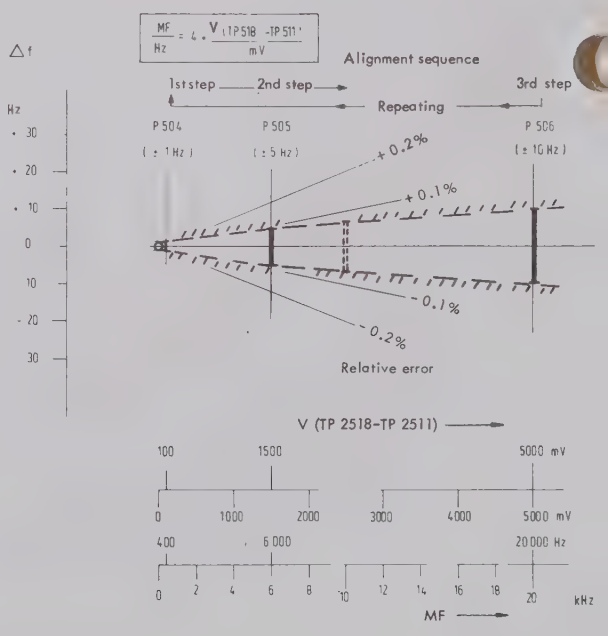


Figure 9-2

9.2.3. Alignment for obtaining equal Comparison Frequencies VF and VF' (P 2502)

Required test equipment: None

Settings on the LD-30:

9. ALIGNMENT INSTRUCTIONS

- Depress pushbutton [28] 3
- Set preselection switch [25] to a low frequency such as 400 Hz.

Alignment Operation:

- Depress pushbuttons [27] and [7] and note the indicated frequency
- Release pushbutton [27] but hold pushbutton [7] down. Frequency ref. freq. is now displayed
- Adjust potentiometer P 2502 until the frequency display agrees with the value noted previously.

9.2.4. Alignment of the Assembly (23) Modulator and Output Amplifier (P 2306)

Required test equipment:
1 Digital voltmeter such as Schlumberger LM 1240.

Preparation:

- Remove identification signal strap c-d on printed circuit board [691-AD] ((24) Modulation Frequency Generation)
- Set operating mode switch [22] to position "MOD Off"
- Set potentiometer [4] to 00.00 kHz (fully anticlockwise) or remove plug from point (23) 1 carrier frequency input on printed circuit board [691-Z]
- Turn potentiometer P 2306 fully anti-clockwise.

9.2.4.1. Offset Alignment of the Modulator Amplifier (P 2304, P 2305)

- Switch [20] to position + 10 dBm
- Remove strap between points (23) 13 and (23) 14 on board [691-Z] ((23) Modulator and Output amplifier)
- Connect point (23) 13 to point (23) 15 (-12 V)
- Connect digital voltmeter to TP 2305 (-) and TP 2306 (+)
- Connect a 100 Ohm resistor between TP 2303 and TP 2304
- Adjust potentiometer P 2305 so that the digital voltmeter indicates less that 20 mV
- Remove 100 Ohm resistor and adjust potentiomer P 2304 for a digital voltmeter indication of ± 1 mV
- Repeat alignment steps 4 to 6 if the digital voltmeter indicates more than 20 mV when the test points TP 2303 and TP 2304 are strapped
- Disconnect the connection between points (23) 13 and (23) 15
- Fit strap (23) 13 and (23) 14
- Replace identification signal strap c-d.

9.2.4.2. Offset Alignment of the Current Amplifier (P 2306)

- Set operating mode switch [22] to position "NORMAL"
- Connect digital voltmeter to TP 2301 (-) and TP 2302 (+)
- Adjust potentiometer P 2306 so that the digital voltmeter indicates 0 ± 0.1 mV
- If the plug was removed from point (23) 1 in the preparations for the test replace it now.

9.2.5. Symmetry Alignment of Modulator II, 41.66 Hz Suppression (P 2308, R 2341)

Required test equipment:

1 W and G distortion analyser KLA-48 or Radiometer wave analyser.

Preparations and settings on the LD-30 Generator.

- Remove identification signal strap c-d on board [691-AD] ((24) Modulation Frequency Generation)
- Remove modulation signal strap b-c on board [691-AA] ((26) Frequency counter) and replace by strap a-c
- Set operating mode switch [22] to position "MOD Off"
- Set test frequency to 00.00 kHz with potentiometer [4] (fully anticlockwise) or remove plug from point (23) 1 (carrier frequency input) on board [691-Z]
- Set switch [20] to position + 10 dBm
- Set potentiometer [5] to position + 1 dBm
- Remove strap from point (23) 13 to (23) 14.

Alignment operation:

- Connect KLA-48 TP 2305 (⊥) and TP 2306 (the measurement can also be carried out at the output, Ra ≤ 10 kOhm)
- Set potentiometer [5] to 0 dBm
- Tune KLA-48 to 41.66 Hz
- The indication on the distortion analyser must be a value between -60 and -70 dB. If this is not the case solder a new resistor R 2341 (1% TK-50 SMA 0207) within the range 14.7 to 750 Ohm (in the E-96 series) between the solder terminals a-b on board [691-Z]

- Set potentiometer [5] to -10 dBm. Adjust potentiometer P 2308 for minimum indication on the distortion analyser (-70 dB is attainable)
- Check the last two steps again to determine whether the values have changed

9. ALIGNMENT INSTRUCTIONS

- Replace signal strap b-c on board 691-AA (26 frequency counter)
- Replace carrier frequency input plug on point 23 1 and the strap from point 23 13 to point 23 14.

9.2.6. Alignment and Test of the Sine-wave Shaper (P 2507, P 2508 P 2509, P 2510

Test configuration:

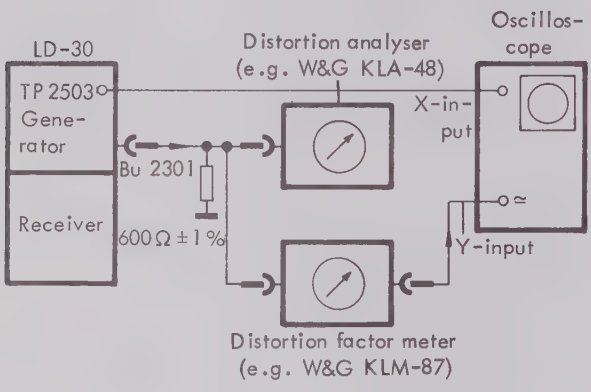


Figure 9-3

Preparations and settings on the LD-30:

- Remove identification signal strap c-d on board 691-AD (24 modulation frequency generation)
- Set operating mode switch 22 to position "MOD Off"
- Measuring frequency: 1 kHz
- Output level: + 10 dBm

Settings on oscilloscope:
- Connect X deflection to TP 2515 (⊥) and TP 2503 (output of saw-tooth generator) in the LD-30 generator and adjust for a horizontal deflection of approximately 10 cm.
- Adjust the Y deflection so that a sine-wave with an amplitude of ± 2 cm is displayed when the distortion factor meter is set to "calibrate" (0.2 V/cm). See also Figure 9-4.

Settings on distortion factor meter:

- Adjust for minimum indication (measuring range: 1%).

Settings on distortion analyser:

- Bandwidth "wide" (calibrated!)
- Adjust the output level of the LD-30 so that the basic frequency of 1 kHz is displayed as +10 dB.

Alignment of k_2 and k_3:

- Locate the second harmonic (2 kHz) on the distortion analyser and adjust potentiometer P 2508 for a minimum indication on the meter (approximately -65 dB)
- Locate the third harmonic (3 kHz) on the distortion analyser. Reduce the indication on the analyser to a minimum (approximately -65 dB) by step by step adjustment of potentiometers P 2507 and P 2508 in opposite directions
- Repeat the preceeding steps several times until k_2 and k_3 remain below -60 dB.

Note:

This alignment operation requires some practice. It is however easily carried out if k_2 is first set to a minimum with potentiometer P 2508, k_3 set "halfway" to the minimum with P 2507, and the remaining distance to the minimum adjusted with potentiometer P 2508 in the opposite direction.
K_2 is then selected again and corrected to minimum with potentiometer P 2508.

Figure 9-5 shows the dependency of the harmonic levels on the settings of potentiometers P 2507 and P 2508.

If the alignment was successful and if all resistors and diodes in the sine-wave shaper are serviceable then the picture shown in Figure 9-4 is obtained on the oscilloscope (with distortion factor meter adjusted, a value of 0.15% = 56 dB).

Adjust potentiometers P 2509 and P 2510 for the minimum deviation from the sine-wave shape even at the peak of the voltage curve, see Figure 9-4. This can also be detected as a minimum in the

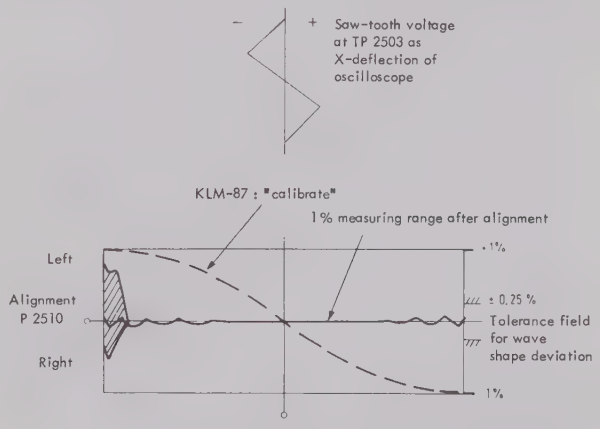


Figure 9-4 Picture of the output voltage on the oscilloscope after subtraction of the basic frequency (= deviation of the voltage curve from the sine-wave shape)

9. ALIGNMENT INSTRUCTIONS

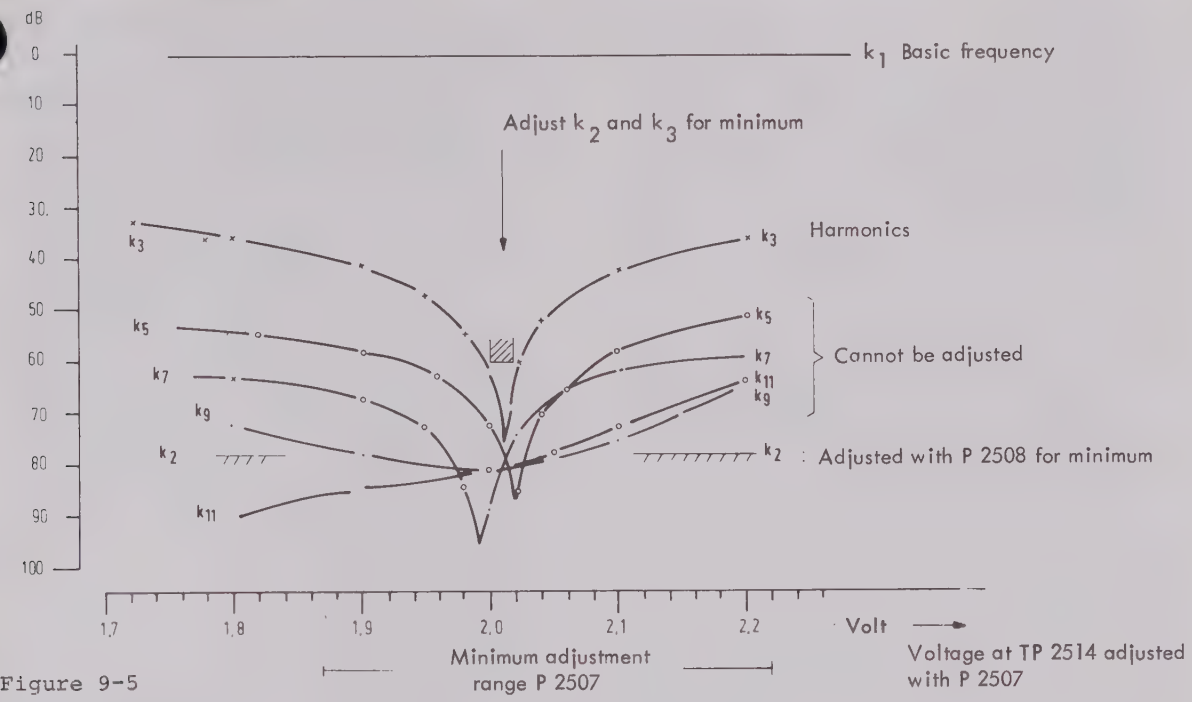


Figure 9-5

indication on the distortion factor meter. Then repeat the first two steps again.

9.2.7. Modulation Distortion and Modulation Factor Alignment on Modulator (P 2302, P 2402)

Required test equipment:

1 Ammeter e.g. Gossen type UM
1 Distortion analyser e.g. W and G KLA-48 or radiometer wave analyser
1 Potentiometer 25 kOhm (carbon-film)
1 Resistor 3.3 kOhm 1/4 W

Preparations and settings on the LD-30:

- Remove identification signal strap b-c on board 691-AD (24 modulation frequency generation)
- Remove modulation strap b-c on board 691-AA (26 frequency counter) and replace by strap a-c
- Set operating mode switch 22 to position "MOD Off"
- Turn potentiometer P 2302 fully clockwise
- Measuring frequency: 1 kHz
- Output level: + 10 dBm

Alignment operation: Modulation distortion

- Connect distortion analyser to the output of the LD-30 and terminate the output of the LD-30 with a matching resistor 600 Ohm ± 1%
- Tune the distortion analyser to the carrier frequency of 1 kHz (bandwidth "narrow", calibrated!)

- The indication on the distortion analyser should be +10 dB. In order to obtain this indication a preliminary adjustment is carried out with potentiometer P 2303
- Remove the strap between point 13 and point 14 on board 691-Z (23 modulator and output amplifier)
- Connection external potentiometer and resistor as shown in Figure 9-6.

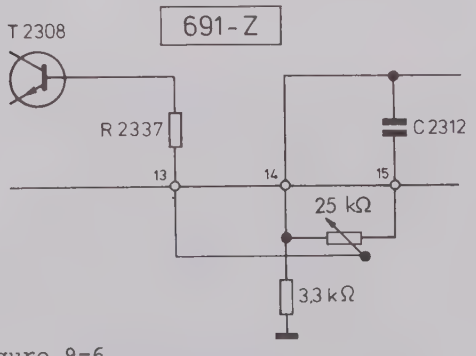


Figure 9-6

9. ALIGNMENT INSTRUCTIONS

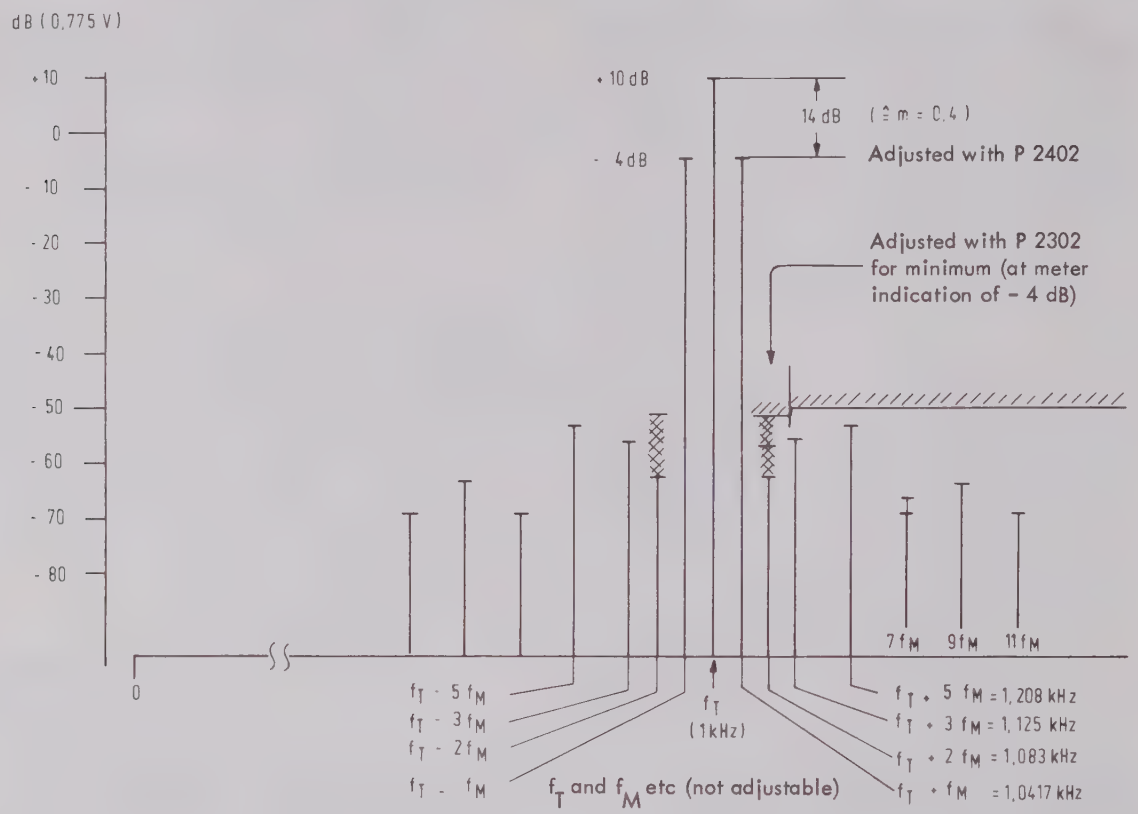


Figure 9-7

- Ammeter is connected between TP 2307 and TP 2308 (+ to TP 2307) and indicates 0.89 mA at + 10 dBm.

The table below shows the appropriate currents for the various output levels.

Level	Current in mA
0 dBm	0.891
- 4 dBm	0.562
-10 dBm	0.282
+ 1 dBm	1.000

Table 9-2

- Turn the external potentiometer until its wiper is at the end connected to point 15. The indication on the distortion analyser must drop to -70dB (-80 dB is attainable). After this adjust the potentiometer again so that the ammeter indicates 0.89 mA.
- Locate the sideband frequency 1.083 kHz (f_T + 2 f_M) on the distortion analyser
- Adjust the external potentiometer so that the ammeter indicates 0.56 mA. Adjust potentiometer P 2302 for a minimum indication on the distortion analyser (approximately -65 dB can be attained)
- Set the current to 0.28 mA and 1.00 mA with the external potentiometer. The indication on the distortion analyser should be less than -52 dB at 1.0 mA and -63 dB at 0.28 mA.

Carry out any necessary corrections with potentiometer P 2302.

Note:

This alignment operation is depicted in Figure 9-7. As the potentiometer P 2302 is adjusted the meter indication of the LD-30 also changes. This operation is shown in Figure 9-8.

Remove the external potentiometer and resistor and replace the strap between point 13 and point 14.

Alignment operation: Modulation Factor.

- Again tune the distortion analyser to 1 kHz (f_T) and set up an output of +10 dB with potentiometer 5
- Locate the sideband frequency 1.0416 kHz (f_T + f_M) on the distortion analyser. The indication should be -4 dB. This can be adjusted with potentiometer P 2402 on board 691-AD (24 modulation frequency generation).

9. ALIGNMENT INSTRUCTIONS

The adjustment range is approximately -7.4 dB to -24 dB.

Subsequent check: Modulation Distortion

- Measure all other sideband frequencies e.g.
  1.083 kHz ($f_T + 2\ f_M$): - 57 dB
  1.125 kHz ($f_T + 3\ f_M$): - 55 dB
  1.208 kHz ($f_T + 5\ f_M$): - 53 dB
  1.291 kHz ($f_T + 7\ f_M$): - 69 dB
  1.375 kHz ($f_T + 9\ f_M$): - 63 dB
- If a value of more than -50 dB is measured for the 3rd and 5th modulation harmonics the components of the pre-distorter R 2301, 2302, 2303, 2306, 2307 and GL 1203 and 2302 must be checked
- Replace the strap between points b-c on board 691-AA
- Replace the identification signal strap c-d on board 691-AD

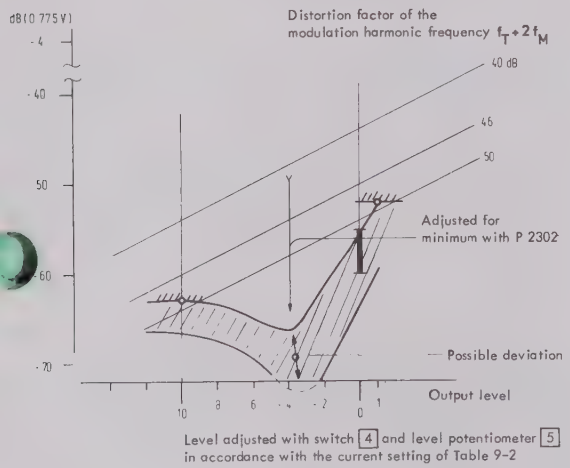

dB(0.775V)
Distortion factor of the modulation harmonic frequency f_T+2f_M
40 dB
46
50
Adjusted for minimum with P 2302
Possible deviation
Output level
Level adjusted with switch 4 and level potentiometer 5 in accordance with the current setting of Table 9-2

Figure 9-8 Level of the sideband frequency $f_T + 2\ f_M$ at the generator output.

9.2.8. Alignment of the Output Level to agree with the Current Input for Remote Control (P 2301, P 2303, P 2311, P2312)

This alignment is necessary in order to obtain the necessary relationships between remote control current and modulator current. The values shown in Table 9-2 show the relationships.

Preparation and settings on the LD-30:

- Set operating mode switch 22 to position "MOD Off"
- Depress pushbutton 28 2
- Measuring frequency: 20 kHz
- Output level: +10 dBm
- Remove strap between point 13 and point 14 on board 691-Z (23 modulator and output amplifier)

Test configuration:

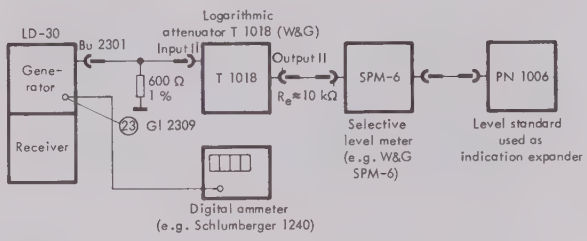


Figure 9-9

- Connect external 25 kOhm potentiometer and 3.3 kOhm resistor as shown in Figure 9-6

Settings on the logarithmic attenuator T 1018:

-Coarse attenuator: 60 dB (in 10 dB steps)
-Fine attenuator: 12 dB (in 1 dB steps)

Settings on the SPM-6:
- $R_i \approx$ 10 kOhm coaxial
- Scale factor x 1
- Bandwidth 0.4 kHz
- Level: -72 dB low-noise
- Frequency: 20 kHz

Settings on Digital Ammeter:

- Measuring range 2 mA and pushbutton "mA" depressed
- Connect ammeter parallel to GL 2309

Alignment operations

- Turn potentiometer P 2301 fully clockwise
- Adjust the external potentiometer for an indication of 0.282 mA on the ammeter
- Set the indication on the SPM-6 to -72 dBm using potentiometer P 2303
- Set the logarithmic attenuator T 1018 to 82 dB
- Setup a current of 0. 891 mA on the digital ammeter using the external potentiometer
- Adjust the indication on SPM-6 to -72 dB with potentiometer 2301
- Set the logarithmic attenuator T 1018 to "72 dB"
- Repeat steps 2 to 6 until no further adjustment is necessary
- Remove the external level potentiometer with resistor and replace the strap between points 13 and 14.

9.2.8.1. Zero Adjustment of the Fine Attenuator Scale

Before aligning the level attenuator it is necessary to check the mechanical

adjustment of the scale on potentiometer [5].

The scale must be readjusted if the scale mark at > +1 dBm of the potentiometer does not agree with the mechanical adjusting point on the cover plate when the potentiometer is turned fully clockwise.

Mechanical Adjustment

- Turn the potentiometer shaft fully clockwise
- Loosen the scale disc on the shaft and turn it until the adjusting mark of the scale between +1 and -6 is exactly above the marker on the front panel to the left of the shaft. Clamp the scale disc in this position. The elongated holes in the scale disc permit exact adjustment of the fine attenuator.

- See Section 7.1.3. for mounting of the knob.

9.2.8.2. Electrical Alignment of the Fine Attenuator Scale

Alignment:

- Set switch [20] to position "10 dBm"
- Set potentiometer [5] to position "0 dBm"
- Set logarithmic attenuator T 1018 to 82 dB
  Adjust potentiometer P 2303 for indication of -72 dB on the SPM-6
- Set potentiometer [5] to position "-6 dBm"
- Set logarithmic attenuator T 1018 to 76 dB
- Adjust potentiometer P 2311 for an indication of -72 dB on the SPM-6
- Set fine attenuator potentiometer [5] to position "0 dB
- Set logarithmic attenuator T 1018 to 82 dB
- Repeat steps 3 to 8 until no further adjustment is necessary
- Set switch [20] to position "+5 dBm"
- Set logarithmic attenuator to T 1018 to 77 dB
- Adjust potentiometer P 2312 for an indication of -72 dB on the SPM-6
- Set switch [20] to position "+10 dBm"
- Set logarithmic attenuator T 1018 to 82 dB
- SPM-6 must indicate -72 dB; otherwise repeat the alignment operations from 3 to 16.

9.2.8.3. Check of the Level Attenuator

- Set switch [20] to position "+10 dBm"
- Set potentiometer [5] to "0 dBm"
- Set logarithmic attenuator T 1018 to 82 dB and the SPM-6 should indicate -72 dB
- Using switch [20] reduce the level from +10 dB in steps of 5 dB
- Reduce the setting of the logarithmic attenuator T 1018 in steps of the same amount and note the deviation from -72 dB on the SPM-6 in each case Permissible deviation in each attenuator position ± 0.05 dB
- Set switch [20] to position "+10 dB"
- Set logarithmic attenuator T 1018 to 82 dB
- Set potentiometer [5] to positions +1 dBm, 0 dBm, -1 dBm to -6 dBm and change the setting of the logarithmic attenuator T 1018 in corresponding 1 dB steps. The level deviation is monitored with the SPM-6 Permissible deviation ± 0.05 dB.

9.2.9. Absolute Level Adjustment of the Output Signal (P 2303)

Test Configuration:

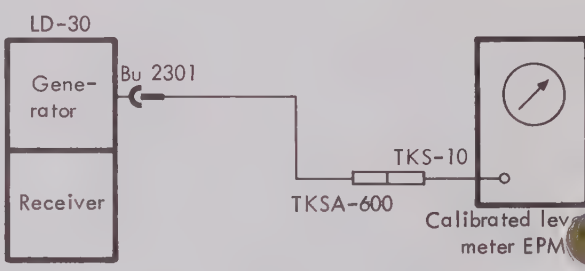


Figure 9-10

The absolute level adjustment of the output signal requires the use of the W and G calibrated level meter EPM-1.

Settings on the LD-30:

- Remove the identification signal strap c-d on board [691-AD] ([24] modulation frequency generation)
- Switch [22] in position "MOD Off"
- Pushbutton [28] 1 depressed
- Measuring frequency: 1.8 kHz
- Output level: 0 dBm

Alignment Operation:

- Calibrate EPM-1 and connect via the series resistor to the output Bu 2301 of the LD-30
- Set potentiometer [5] exactly to "0 dBm"
- Adjust potentiometer P 2303 for an indication of exactly "0 dBm" on the EPM-1
- Remove the signal strap b-c on board [691-AA] ([24] modulation frequency generation) and replace by strap a-c
- The indication on the EPM-1 must increase by 0.334 dB
  Tolerance + 0.326 to + 0.342 dB

9. ALIGNMENT INSTRUCTIONS

- The modulation factor set up in step 9.2.7. (m = 0.4) is checked by this measurement
- If the above tolerances are not maintained potentiometer P 2402 on board 691-AD (24 modulation frequency generation) must be readjusted
- Move the strap a-c on board 691-AA to b-c. Replace c-d on board 691-AD

9.2.10. X-Output, Offset, Linearity (P 2511)

The test configuration and the alignment are described in Section 9.3.7.

9.2.11. Alignment of the Additional Cards

9.2.11.1. Remote Control Device BN 691/11

The remote control device consists of the boards:

Measuring frequency remote control
Buffer for level remote control
Reference frequency remote control

Functional check of the measuring frequency remote control

Required test equipment:

1 test set LD-30

Test Configuration:

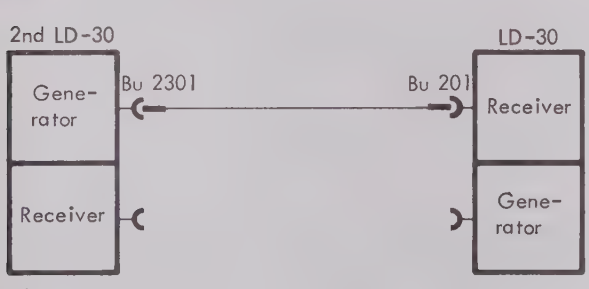


Figure 9-11

Settings on the LD-30 (with remote control)

- Switch 22 in position "NORMAL"
- Switch 8 in position " GENERATOR"

Functional Check:

- Vary the measuring frequency with potentiometer 4 and the indication 9 must change accordingly
- Set switch 22 to position "Remote Control"
- Vary the measuring frequency with potentiometer 4 ; in this case the indication 9 must not change

Settings on the 2nd LD-30:

- Switch 22 in position "NORMAL"
- Switch 8 in position "GENERATOR"
- Measuring frequency: 20 kHz
- Reference frequency: 400 Hz
- Connect Bu 2301 to Bu 201
- Check the values of the measuring frequencies with the switch 8 set to positions " GENERATOR" and receiver. Required value: ± 2 Hz.

Functional check of the remote control device:

- Connect Bu 2301 on 2nd test set to Bu 201 on the LD-30 being tested
- Switch 8 on the LD-30 to position "GENERATOR"
- Switch 22 on the LD-30 to position "Remote Control"
- Compare the indication 9 on the LD-30 being tested with the indication 9 on the 2nd test set; required value: ± 2 Hz.

9.2.11.2. A.F. Dialling Block BN 691/12

Alignment instructions for the operating point of the step frequencies can be found in Section 5.3.2. of the Description and Operating Instructions.

9.3. RECEIVER

9.3.1. Supply Voltages

See Section 9.1.

9.3.2. Alignment of the working points of the Input Amplifier (P 201, P 202)

Required test equipment:

1 Digital voltmeter such as H + B T 2000.

Operational generator in the LD-30 being tested.

Preparation and settings:

- Connect generator output to receiver input
- Output level: 0 dBm
- Measuring frequency: 1.8 kHz
- Reference frequency: 1.8 kHz
- Receiver settings immaterial
- Measure the DC voltage at test point TP 201 with reference to ground and adjust to -6 V with potentiometer P 201
- After this adjust the voltage at TP 202 to -6 V using P 202
- The voltage difference between the two test points should not be greater than 10 mV.

9. ALIGNMENT INSTRUCTIONS

9.3.3. Meter Zero (P 304) and Full Scale Deflection (P 303)

9.3.3.1. Mechanical Zero

With the test set switched off and standing on a horizontal surface the pointer of the meter must indicate 0. If necessary the pointer can be carefully adjusted with the screw below the meter.

9.3.3.2. Electrical Zero

Required test equipment:

1 Digital voltmeter such as H + B T 2000.

Connect the output of the generator to the input of the receiver.

Settings on the LD-30 generator

Output level: 0 dBm
- Measuring frequency: 1.8 kHz
- Reference frequency: 1.8 kHz

Settings on the LD-30 receiver

- Set switch [23] to "± 50 dB"
- Pushbutton [31] 4 depressed
- Pushbutton [31] 6 not depressed
- Measure the voltage at Bu [34] with a digital voltmeter and adjust potentiometer P 304 for a DC voltage of 0 V.

9.3.3.3. Full Scale Deflection

- Pushbutton [31] 2 depressed
- Adjust potentiometer P 303 so that full scale deflection (scale mark +5) is indicated on the meter [10].
- Measure +2.5 V with the digital voltmeter at Bu [34].

9.3.4. Level Indication (P 203, P205, P 302)

The test configuration and settings of the equipment are as described in Section 8.6. Before starting this alignment the LD-30 should have been switched on for approximately 1 hour. Check each output level with the PM-8 and then connect it to the input of the LD-30.

Carry out the alignment in accordance with the following plan:

Set potentiometer [5] exactly to position 0 dBm.

Output level switch [20]	Switch [33] in position	Potentiometer	Align for meter indication [1]:
0 dBm	0 dBm	P 203	0
-10 dBm	0 dBm	P 205	-10 (f.s.d.)
+10 dBm	0 dBm	P 207	+10 (f.s.d.)
-20 dBm	-20 dBm	P 302	0

9.3.5. A.G.C. Amplifier, Schmitt Trigger (P 501)

Test Configuration:

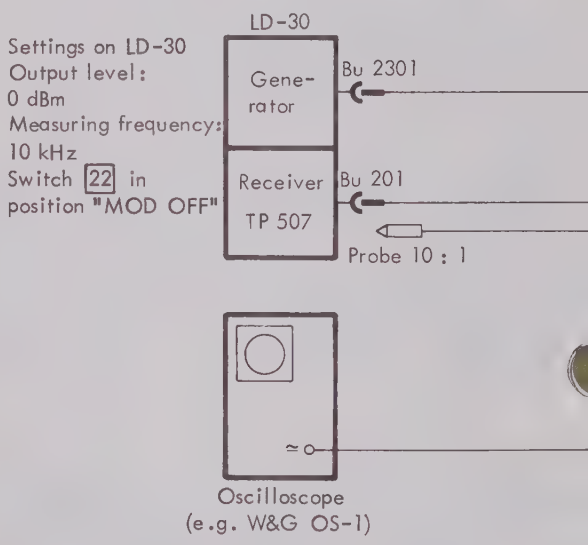


Figure 9-12

- Measure with an oscilloscope on test point TP 507 with respect to ground and adjust P 501 until the pulse duty cycle of the square-wave signal is 1:2 (equal sized rectangles).

9.3.6. Check of the Frequency Evaluation Circuit

Settings on the OS-1

- Vertical: 0.1 V/cm
- Horizontal: 100 µs/cm
- Trigger: internal

1) Reading the meter can be omitted if the test configuration shown in Section 8.5 is used.
Repeat the alignment at output levels 0, - 10, and +10 dBm several times before executing the alignment for -20 dBm. After each interruption of the signal, wait a few seconds until the indication has settles to its final value.

9. ALIGNMENT INSTRUCTIONS

Test Configuration:

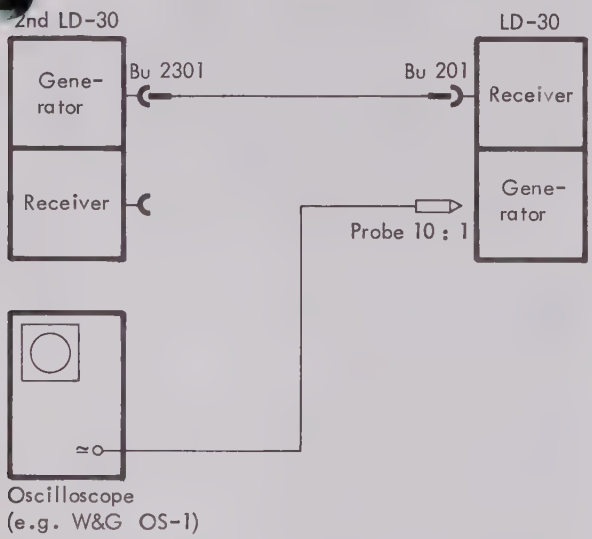


Figure 9-13

Settings on the LD-30 (2nd unit)

- Switch [8] in position "GENERATOR"
- Output level: 0 dBm
- Measuring frequency: 2 kHz
- Switch [22] in position "MOD Off"

9.3.6.1. Check of the Level Constancy at TP 502

- Connect OS-1 to TP 502
- Vary the output level on the 2nd LD-30 from +10 dBm to -50 dBm
- Required value: 4 V_{pp} to 5 V_{pp}

9.3.6.2. Check of the Frequency Variation at TP 507

- Connect OS-1 to TP 507
- Output level on 2nd LD-30: -50 dBm
- Vary the measuring frequency: 200 Hz to 20 kHz.

The amplitude and pulse duty cycle at TP 507 must remain constant. Adjust the horizontal deflection of the oscillo - scope to suit the measuring frequency.

9.3.7. X-Outputs Bu [35], Linearity, Offset (P 2511, P503)

Settings on the LD-30:

- Pushbutton [31] 2 depressed
- Pushbutton [28] 3 depressed
- Pushbutton [3] depressed, set USL 20 kHz
- Pushbutton [18] depressed, set LSL 200 Hz

Test Configuration:

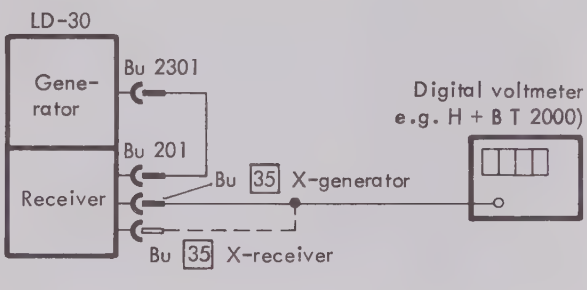


Figure 9-14

Connect digital voltmeter to Bu [35] "X-SEND.FREQ."

Alignment:

- Adjust potentiometer P 2511 for indication of 50 mV ± 1 mV on the digital voltmeter
- Depress pushbutton [3] The indication on the digital voltmeter must be the required value 5 V ± 50 mV
- Note the digital voltmeter indications at LSL and USL
- Connect digital voltmeter to Bu [35] "X-REC.FREQ."
- Adjust potentiometer P 503 for a digital voltmeter indication which differs from the noted value by not more than ± 50 mV
- Depress pushbutton [18]
- Compare the indication on the digital voltmeter with the noted LSL value, the difference is not more than 0.5 mV with respect to the noted value.

9.3.8. Delay 70 ms (P 305)

Test Configuration:

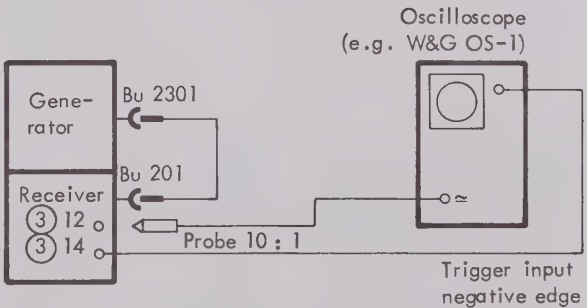


Figure 9-15

Generator setting:

- Output level: 0 dBm
- Any frequency

9. ALIGNMENT INSTRUCTIONS

Receiver setting:

- Pushbutton [31] 5 depressed
- Switch [33] in position " 0 dBm"
- First connect trigger signal (4.16 Hz) from TP 301 to the Y-input of the oscilloscope and adjust the horizontal deflection of the oscilloscope so that one complete cycle of the trigger signal is displayed over a width of 10 cm on the screen
- Then display the signal at point ③ 12 and adjust potentiometer P 305 for a pulse width of 50 ms (≅ 21 mm). See Figure 9-16.

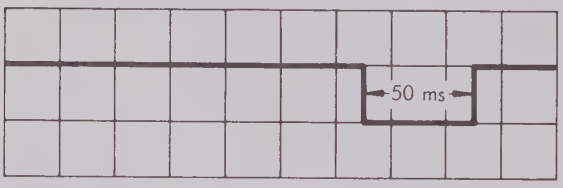


Figure 9-16

With this setting the alignment of the 70 ms delay of IC 304/2.1 is correctly carried out (120ms - 50ms = 70ms).

9.3.9. Split Frequency Filter, Attenuation Peaks (P 401, P 402)

Test Configuration:

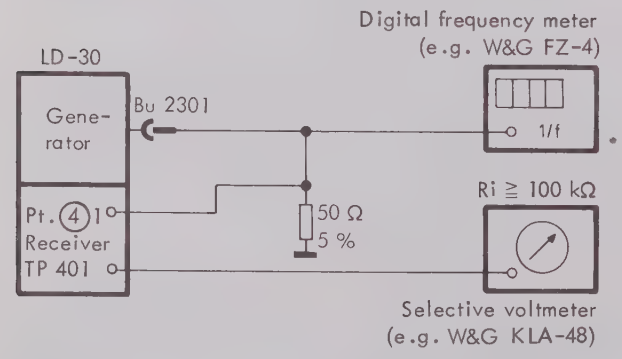


Figure 9-17

Generator setting:

- Switch [22] in position "MOD Off"
- Output level: +6.5 dBm

Note:

The connection from the logarithmer ② 13 to connection point ④ 1 must be removed.

- At a generator frequency of 125 Hz (1/f = 8 ms) the filter attenuation is adjusted to maximum with P 401.
- In a similar manner the attenuation peak at 83.3 Hz (1/f = 12 ms) is adjusted for maximum with P 402.

Note:

The LD-30 generator can be used down as far as the lower peak frequency (83.3 Hz) for this alignment.

9.3.10. Zero-Transition Detector (P 403)

Required test equipment:

1 Oscilloscope with 10 : 1 probe such as W and G type OS-1.

- The connection from the logarithmer ② 13 to the connection point ④ 1 must be removed
- Connect test point TP 403 to ground
- Connect oscilloscope to TP 402 and display the DC voltage
- First set potentiometer P 403 fully anticlockwise. The voltage at TP 402 is now approximately +5 V. Then turn potentiometer P 403 slowly clockwise until the voltage suddenly jumps to 0 V. This is the correct setting of potentiometer P 403.
- Care should be taken that the voltage jump from 0 V to +5 V is not selected. This is important as the comparator has a hysteresis of 5 mV and the subsequent circuit evaluates the signal edge from +5 V to 0 V.
- After this adjustment remove the ground connection from TP 403 and replace the connection from the logarithmer ② 13 to the input of the edge filter ④ 1.

9.3.11. Checking the 100 ms monostable (P 406)

Test Configuration :

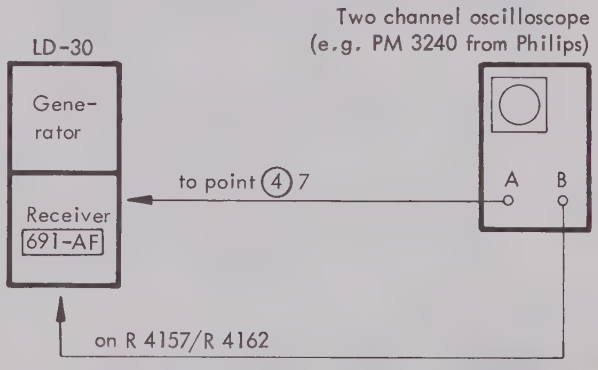


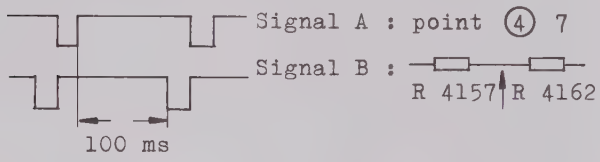
Figure 9-18

Settings on oscilloscope
- Horizontal : 10 ms/div

9. ALIGNMENT INSTRUCTIONS

Vertical: 2 V/div
Triggers at positive transitions of channel A

- Calibrate oscilloscope by means of 100 ms gate time at TP 2404
- Finally measure at the points given in Fig. 9-18, the following pulse plan shows which transitions of the pulses displayed on the CRT screen should be at 100 ms intervals.



- Use potentiometer P 406 to adjust for 100 ± 0.5 ms.

9.3.12. Group Delay Indication (P 301, P 405)

Before carrying out this alignment the 100 ms delay should be checked in accordance with Section 9.3.11. (also necessary for units with crystal time base).

Test Configuration:

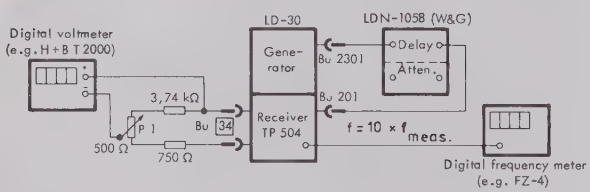


Figure 9-19

Note:
Before carrying out alignment check that the mechanical and electrical zero of the meter and its full scale deflection are correct (see Section 9.3.3.)

Settings on LD-30 generator
- Output level: 0 dBm
- Measuring frequency: 1.271 kHz
- With pushbutton 27 depressed adjust the reference frequency to 2.031 kHz ± 2 Hz using switch 25 and potentiometer 26 .

It should also be noted that the connected digital frequency meter indicates 10 times the actual reference or measuring frequency (20. 31 or 12. 71 kHz respectively).

Settings on the LD-30:

- Pushbutton 31 2 depressed, set indication on digital voltmeter to 1000 mV with voltage divider
- Pushbutton 31 3 depressed
- Switch 11 in position "± 0.5 ms"
- Pushbutton 31 6 depressed

Determine the delay zero error:

- Depress pushbutton 27 on the LD-30 and read off the zero error (N) on the digital voltmeter.
  Value of the zero error: 0 to -8 mV (≅ 0 to -4 µs).

Align delay indication:

- Release pushbutton 27 and adjust potentiometer P 301 so that the digital voltmeter indicates +1000 mV +N.

Example: Actual zero error: -6 mV (≅ -3 µs)
Value to which indication must be adjusted:
+1000 mV -6 mV = +994 mV
(+500 µs -3 µs = +497 µs)

Alignment of the basic delay shift 10 ms add 5 ms:

- Set switch 11 to position "±10 ms"
- Depress pushbutton 27 , read indication on digital voltmeter and record it
- Set switch 11 to position "±10 ms add 5 ms". Adjust potentiometer P 405 until the indication shift with respect to the previously recorded value is -500 mV ±1 mV.

9.3.13. Check of the Speech Channel

9.3.13.1. Check with Microphone "2-Wire Input"

Test Configuration:

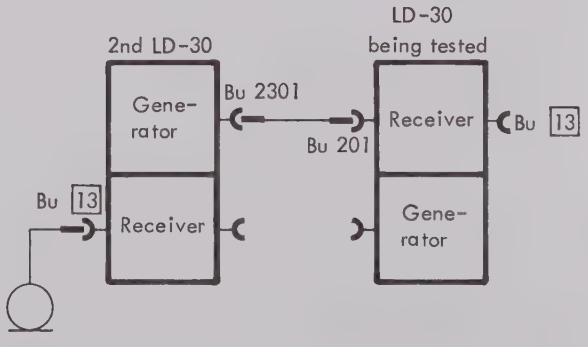


Figure 9-20

9. ALIGNMENT INSTRUCTIONS

Settings on 2nd LD-30

- Output level 0 dBm
- Any frequency
- Pushbutton [29] 1 depressed
  (Switch [22] in position "Speech")
- Connect microphone to Bu [13]

Settings on LD-30 being tested

- Output level 0 dBm
- Any frequency
- Pushbutton [29] 2 depressed
- Switch [22] in position "NORMAL"
- Connect a strap between point 4 and point 5 on Bu [13]
- Turn up volume with potentiometer [30]

When speaking into the microphone the speech signal is audible in the loudspeaker and the existing test signal is muted.

9.3.13.2. Check of "2-Wire Output"

Test Configuration:

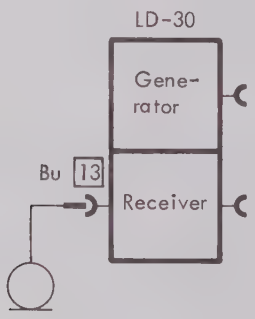


Figure 9-21

Settings on LD-30:

- Level 0 dBm
- Any frequency
- Switch [29] 1 depressed
- Volume turned up with potentiometer [30]

The speech signal coming from the microphone is audible in the loudspeaker of the unit being tested.

9.3.13.3. Alignment of the "230 ms Single Shot"

Settings on the OS-2:

- Triggered internally to the edge of the 20 ms pulse at TP 601
- Pushbutton A + B depressed
- Horizontal 5 ms/cm
- Vertical 2 V/cm

Settings on the LD-30

- Switch [22] in position "NORMAL"

Test Configuration:

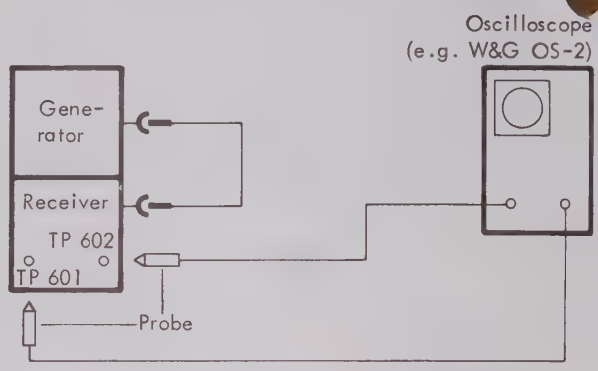


Figure 9-22

- Output level: 0 dBm
- Pushbutton [29] 2 depressed
  Check the 20 ms single shot
- Ti = 20 ms ± 4 ms

Alignment:

- Switch OS-2 to
- Horizontal: 2 ms/cm
- Vertical: 2 V/cm
- Adjust the 20 ms pulse to a length of 80 mm

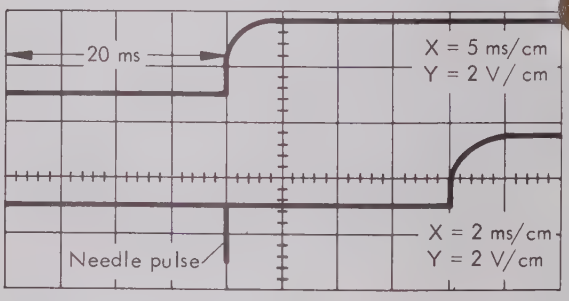


Figure 9-23

- Adjust potentiometer P 603 until the needle pulse is in the centre of the 20 ms pulse
- Set switch [22] to position "GENERATOR Off" and return it to "NORMAL". With potentiometer [30] turned up the volume of the audible signal in the loudspeaker must be reduced after approximately 2 s. The "low level" can be adjusted with the aid of potentiometer P 604.

9.3.14. Alignment of the Additional Parts

(See also Section 5.3.1. of the Description and Operating Instructions).

9. ALIGNMENT INSTRUCTIONS

9.3.14.1. Buffer for Level Remote Control BN 691/11 (P 1101, P 1102, P 1104

Test Configuration:

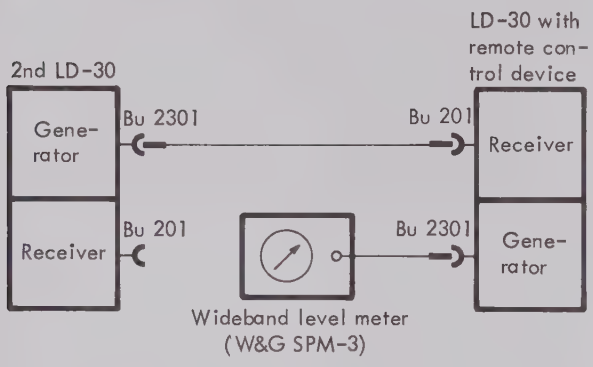


Figure 9-24

Settings on the LD-30 with Remote Control

- Switch [22] in position "Remote Control"
- Switch [20] and potentiometer [5] in position "0 dBm"
- Pushbutton [31] 5 depressed
- Switch [33] in position "0 dBm"

Alignment:

- Adjust the output of the 2nd LD-30 with switch [20] and potentiometer [5] until the receiver of the LD-30 being tested indicates 0 dBm.
- Adjust potentiometer P 1102 until the indication on the SPM-3 is 0 dBm.

Carry out this check in a similar manner at -30 dBm and adjust with potentiometer P 1104.

Alignment of the compensation of the input current of IC 1101.

Test configuration and equipment settings as above.

- Select output level -30 dBm and note the indication on the digital voltmeter
- If the junction of R 1118/R1119 (see Figure 9-25) is connected to ground the indication on the SPM-3 should not change (< 0.1 dB) for a period of approximately 5 s.

If the level becomes larger or smaller carry out the following adjustment:

Remove the ground connection
Adjust P 1101 slightly
Note the new level
- Connect the ground connection
- Determine the change in the level
- The direction and amount of potentiometer adjustment and the resulting level variation can now be used to determine how the potentiometer must be adjusted for further steps
- It may be necessary to repeat the above operation several times until the specification is fulfilled.

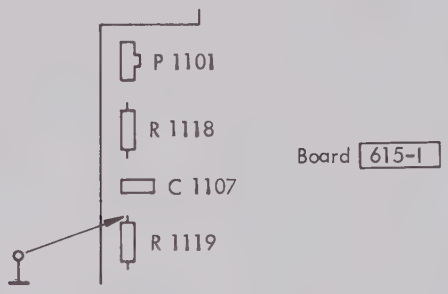


Figure 9-25

9.3.14.2. Reference Frequency Discriminator BN 691/11 (P 1201, P 1202)

Test Configuration:

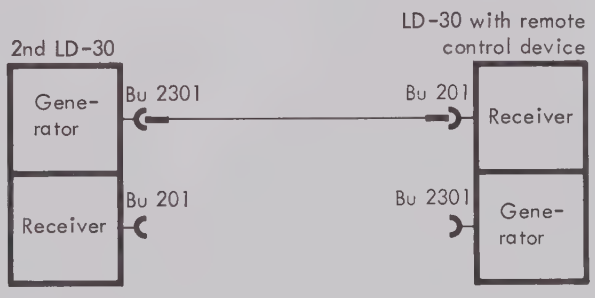


Figure 9-26

Before starting the adjustment the LD-30 should have been switched on for at least 30 minutes with the additional card fitted.

Settings on the 2nd LD-30

- Switch [8] in position "GENERATOR"
- Switch [22] in position "MOD Off"
- Output level: 0 dBm
- Reference frequency: 20 kHz ± 10 Hz

Settings on the LD-30 with remote control device

- Switch [8] in position "GENERATOR"

Alignment:

- Depress the pushbutton [27] on the 2nd LD-30

- Adjust potentiometer P 1202 on board 615-K1 so that the indication [9] on the LD-30 shows the same frequency as in the position " Receiver" of switch [8]
  Pushbutton [7] should remain depressed for 1 Hz resolution.

The measurement is also carried out at the 0.4 kHz and any necessary adjustments carried out with potentiometer P 1201.

9.3.15. Alignment Operations which are not carried out

The following alignment operations require more test work or special test equipment and can therefore be carried out only in the factory:

1. Evaluation circuit (4)
   Operating point of the identification pulse (P404).
2. Input amplifier (2) (logarithmer)
   Delay alignment when attenuation difference also present (P 204).

10. DESCRIPTION OF FUNCTION

10. DESCRIPTION OF FUNCTION

The appendix for the servicing instructions with the block diagram and circuit diagrams should be used as a further aid for understanding the following sections. In the detailed descriptions of the assemblies the numbers in parentheses in the section headings refer to the numbers of the circuit diagrams in the appendix.

10.1. FUNCTION OF THE TEST SET ON THE BASIS OF THE BLOCK DIAGRAM

The method of operation and functions of the generator and of the receiver LD-30 are sufficiently described in Chapter 4 "Functions and Characteristics" of the Description and Operating Instructions.

10.2. DETAILED DESCRIPTION OF THE GENERATOR ASSEMBLIES

10.2.1. Carrier Frequency Generation (25)

The carrier frequency generation circuits can be divided into four functional groups.

Carrier frequency switch and saw-tooth generator
Sine-wave shaper
Signal generation
Frequency control (sweep control)

10.2.1.1. Carrier Frequency Switch, Saw-Tooth Generator

The carrier frequency switch consists of three field-effect transistors T 2519 to T 2521 which are controlled by the logic circuit IC 2518, IC 2517 and IC 2516. Depending on the operating mode - continuous ≙ modulation off or alternating ≙ switched modulated signal - the control differs. The selection of the control is carried out by suitable switching of the FET switches.

Continuous:
In this mode the input of the NAND-Circuit IC 2518/3.1 point (25) 21 has a " 1" ≙ 0 V signal. This means that transistors T 2523/T 2524 are caused to conduct and T 2522 is cut off by the logic circuit. This in turn means that the FET switch for the reference frequency Ref.Freq. (T 2520) and for the external reference frequency Ref.Freq. ext. (T 2521) is cut off and the FET switch for the measuring frequency MF (T 2519) conducts. Connected of an external reference frequency has no effect in this operating mode.

Alternating:
In this mode the input of the NAND - circuit IC 2518/3.1 point 21 has a "0" ≙ + 5 V signal. The 4.16 Hz "a" switching signal available at point (25) 22 is now effective and switches the FET switches T 2519 (MF) and T 2520 (Ref.Freq.) alternately on (conducting) and off (cut off) in the rhythm of the 4.16 Hz signal via the logic circuit and the control transistors T 2522 and T 2523.

If an external reference frequency Ref. Freq. ext. is now connected then this has priority. The switching in the 4.16 Hz rhythm is now carried out between FET switches T 2519 and T 2521 i.e. between MF and Ref.Freq. ext. The FET switch T 2520 is cut off by the control logic.

If in this mode the position "Remod." (retransmission) is selected then the logical relationships are changed as follows: A 1 signal (0 V) is applied to the input of the NAND - circuit IC 2518/3.2, this signal being controlled by the circuit modulator and output amplifier (23), (T 2313).

If the Ref.Freq. ext. is simultaneously present the FET switches T 2519 (MF) and T 2520 (Ref.Freq.) are cut off, T 2521 (Ref.Freq. ext.) conducts. If the external Ref.Freq. is now interrupted FET switch T 2521 is cut off and T 2520 conducts.

The DC voltage signal available at the output of the FET switch is passed to the current source IC 2519 and T 2529 of the saw-tooth generator.

The basic construction of the saw-tooth generator for generation of a saw-tooth wave form is shown in Figure 10-1.

The current source impresses on the saw-tooth generator a charging current for C 2525 which is proportional to the voltage.

The upper frequency limit is adjusted, with the appropriate voltage applied, with potentiometer P 2505 and the lower frequency limit with potentiometer P 2504.

Table 10-1 shows the relationships between frequency and voltage.

Input voltage at IC 2519	Reference voltage TP 2517 with respect to + 7.7 V	Output frequency corresponding to voltage
7.75 V	50 mV	f = 200 Hz
2.75 V	5 V	f = 20 kHz

Table 10-1

10. DESCRIPTION OF FUNCTION

The positive voltage coming from the emitter of transistor T 2525 cuts off T 2530 and T 2531 conducts. In addition T 2526 conducts and also causes T 2532 to conduct. Transistor T 2533 is cut off. The rising flank of the saw-tooth wave form is now generated (current flow shown by dotted arrow in Figure 10-1). The saw-tooth signal is extracted at the collectors of T 2531/T 2533 and passed via the impedance stages T 2536/T 2537 and T 2540 to the comparators IC 2520/ IC 2521. When the negative input of IC 2520 becomes more positive than +3.75 V comparator IC 2520 switches and changes the state of the RS-flip-flop IC 2517. The transistors in the saw-tooth generator are reversed (T 2530/ T 2533 conducting, T 2531/ T2532 cut off). The falling flank of the saw-tooth wave form is now generated (current flow shown by solid arrow in the figure). As the minimum charging current is approximately 60 µA the coupling stages T 2536/ T 2537 and T 2528/T 2527 are designed as Darlington stages in order to avoid linearity errors in the saw-tooth wave form.

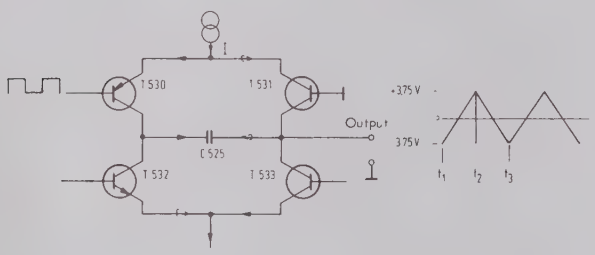


Figure 10-1 Basic circuit diagram of the saw-tooth generator and saw-tooth voltage wave form from t_1 to t_3.

The comparators IC 2520 and IC 2521 with the RS-flip-flop IC 2517/4.3 supply pulses for control of reversing of the charging direction. The saw-tooth wave form reaches +3.75 V at time t_2 (see Figure 10-2). At this point the comparator IC 2520 switches to "1" and sets flip-flop IC 2517. Comparator IC 2521 switches at point t_1.

At the output of flip-flop IC 2517 the signal for reversing the charging direction is passed to the 10 x multiplier circuit and frequency evaluation (5) in the frequency counter (26).

The current source T 2542 is used to add, via R 25186/C 2531 in series with the Zener diode GL 2520, a voltage step with a positive or negative direction, depending on the position of RS-flip-flop IC 2517, to the inverter IC 2522. The current source T 2542 is frequency dependent. The base voltage varies proportionally with the frequency. Transistor T 2541 is necessary in order to avoid a frequency response error due to high base current.

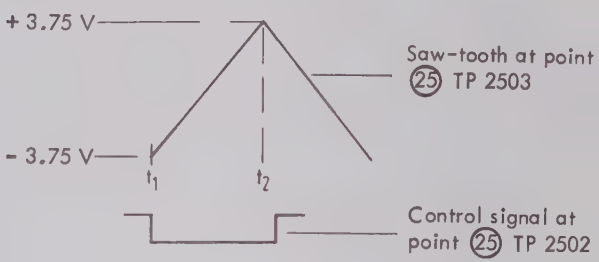


Figure 10-2 Charging direction reversing pulse.

The sine-wave shaper and the 10:1 divider in the 10 x multiplier in the frequency counter (26) are fed from the reference voltage (GL 2520).

10.2.1.2. Sine-Wave Shaper

The saw-tooth wave form coming from the saw-tooth generator is converted into a sine-wave signal.

The sine-wave shaper operates on the principle of a diode function generator. The sine-wave function is achieved by the addition of tangents with varying angles of steepness.

The saw-tooth signal is extracted at the output of the impedance stage T 2539/ T 2540 and fed to the sine-wave shaper via the internal resistor R 25200/1 kOhm. The circuit with the diodes GL 2526 to GL 2532 is used for shaping the positive half-cycle and the circuit with the diodes GL 2533 to GL 2539 for the negative half-cycle. The two transistors T 2547 and T 2548 form the voltage source for the dividers.The break points of the characteristics can be adjusted with potentiometers P 2507 and P 2508 in order to reduce the destortion factor of the output signal to a minimum.

During sine-wave shaping the break points are rounded off to a greater degree by the diodes. An additional peak compensation which can be adjusted with the potentiometers P 2509 and P 2510 is also provided.

10.2.1.3. Signal Generation

The signal generation circuits contain the preparation of the 7.7 V reference voltage, the settings for the upper and lower sweep limits and the setting for the reference and measuring frequency. These settings are all purely DC voltages. They are varied within certain limits and are later converted into a frequency in the saw-tooth generator circuit.

The 7.7 V is generated by means of the voltage divider R 2525/R 2526. The regulation circuit with IC 2503 and T 2502 ensures that the 7.7 V reference voltage is available with suitable regulation at TP 2513.

A further very important voltage is the 3.8 V between TP 2505 and TP 2513. This results from the difference between 11.5 V at TP 2505 and 7.7 V at TP 2513. The 3.8 V difference voltage is adjusted with P 2501. The filter circuit with IC 2501 and T 2501 removes interference voltages on the supply lines and thus prevents the generation of frequency modulation.

10.2.1.3.1. Measuring Frequency Adjustment

The measuring frequency adjustment is carried out continuously with potentiometer P 2503 via the regulation circuit IC 2510, IC 2511, T 2509, T 2513 and IC 2512 (see Figure 10-3). The selected frequency is displayed directly on the frequency display. The resolution is 10 or 1 Hz.

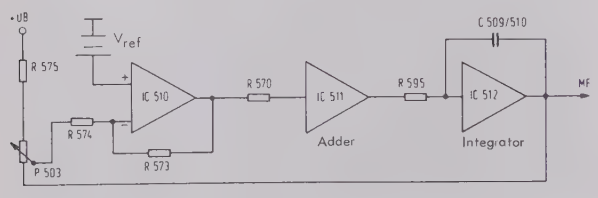


Figure 10-3

According to the setting of potentiometer P 2503 the voltage at the output of the integrator varies. The voltage range is betwen 2.7 V and 7.65 V.

The regulation circuits for the upper sweep limit with IC 2506, IC 2511, T 2509, T 2513, and IC 2512, for the lower sweep limit with IC 2507, IC 2511, T 2509, T 2513, and IC 2512 and for the reference frequency with IC 2509, IC 2508, IC 2511, T 2509, T 2513, and IC 512 are constructed in a similar manner.

There is a small difference only in the circuit for the reference frequency. In this regulation circuit there is an output on integrator IC 2512 (measuring frequency) and a direct output at IC 2509 (reference frequency). The reference frequency is adjusted in steps of 10 Hz, 100 Hz and 1 kHz with S 2203. IC 2502 is also connected to the measuring frequency line in order to convert the frequency proportional voltage to 0...+5V for connection of an X-Y recorder.

10.2.1.3.2. Reference Frequency Adjustment

The reference frequency can be adjusted in 100 Hz steps from 200 Hz to 19.9 kHz on the front panel. The adjustment is carried out by means of the decade switch [25] which is designed as a resistance divider. The selected frequency is displayed on the frequency display when pushbutton [27] is depressed. Exact adjustment of the frequency can be carried out with the calibration potentiometer [26].

When pushbutton [27] is depressed a 1-signal (0 V) is applied to GL 2508 via the logical circuit formed by IC 2529/ 2.1 and IC 2527/ 4.2. This cuts off transistor T 2505 and the regulation switches on. The integrator output IC 2512 changes to the adjusted voltage. The regulation circuits for the upper and lower sweep limits are inactive. The regulation circuit for the means.rrequency is switched off when pushbutton [27] is depressed. This means that transistors T 2503, T 2504, and T 2506 are activated via the appropriate logic circuits and 0-signal (7 V) is applied to the cathodes of GL 2505, GL 2506, and GL 2510. If the alternating mode of operation is selected, switching between MF and Ref.Freq. or Ref.Freq. ext. is suppressed. Similar operations are carried out when the pushbuttons for the upper and lower sweep limits are depressed. In each case one of the four transistors T 2503 to T 2506, corresponding to the operated pushbutton, is cut off (regulation circuit activated). All other transistors conduct (regulating circuit switched off). If none of the three pushbuttons is depressed the measuring frequency "MF" is activated.

The operations described above are active only when the pushbuttons [28] 3, 4, are not depressed. In the operating mode sweep ⌒ or sweep ⌒ a 0-signal (5 V) is applied to GL 2510 and transistor T 2506 conducts. This causes all transistors T 2503 to T 2506 to conduct until a sweep limit is reached and the

regulation for the upper and lower sweep limit is switched on again.

At the same time a O-signal (5 V) is applied via GL 2503 to IC 2513/6.1. This means that there is a 1-signal at the output of IC 2513/6.2. Transistors T 2507/T 2508 thus conduct and T 2509 is cut off. The signal at IC 2514/4.1 pin 5 has no effect in this case.

It should also be mentioned that a 1-signal (O V) on the two inputs of the gate circuit IC 2513/2.1 and IC 2531/2.2 cuts off transistors C 2511/C 2510. The gate circuit is controlled by T 2555 (O-signal +5 V on the collector).

Splitting of,the reference frequency Ref.Freq. into a direct transmission path and a path via the regulation circuit of the measuring frequency MF is necessary for two operating modes. In the mode "NORMAL" the selected Ref.Freq. is fed directly via IC 2509 to switch T 2520 and the MF via the main regulation circuit mentioned above to switch T 2519. The switches T 2519/T 2520 are switched on and off in the 4.16 Hz rhythm and the applied voltage values are fed to the saw-tooth generator. If the MF and Ref.Freq. were only fed via one main regulation circuit then this would have to settle to a new voltage value in each of the 4.16 Hz periods according to the selected MF and Ref.Freq.

If the Ref.Freq. is to be measured with the frequency counter the Ref.Freq. automatically switches itself into the main regulation circuit of the MF when pushbutton [27] is operated.

Frequency measurement with the internal frequency counter is always carried out in the measuring time during a period of 100 ms (gate time). This measuring circuit is necessary in order to prevent the counter from switching between MF and Ref.Freq. in the 4.16 Hz rhythm and to ensure that only the MF or the frequency connected into the MF channel is displayed. If the pushbutton [27] is depressed switch T 2520 cuts off. The Ref. Freq. voltage is now fed through the main regulation circuit of IC 2508 to the output of integrator of IC 2512 and is thus fed into the MF channel. Switch T 2519 is energised via the switch control and conducts. The Ref.Freq. is now displayed.

In the mode "MOD Off" (continuous signal without modulation) it is possible to send four fixed frequencies.

If one of the pushbuttons [3], [18], or [27] is depressed the output frequency jumps from the MF to the preselected value and appears on both the frequency display and at the output of the generator. The frequency is available only while the pushbutton is depressed.

If however the pushbutton [28] 3 is depressed it is necessary to operate pushbutton [3], [18], or [27] only momentarily. The appropriate selected frequency is now available at the output of the generator and is displayed on the frequency counter when the pushbutton is released. If the pushbutton [28] 3 is released by pushbutton [28] 1 or [28] 2 the frequency returns to the selected MF.

10.2.1.4. Frequency Control (Sweep Control)

The sweep mode is selected with pushbuttons [28] 3 single sweep and [28] 4 continuous sweep.

The sweep rate is selected for all sweep modes with switch [19].

10.2.1.4.1. Single Sweep

When a preset sweep limit is reached the sweep is switched off. The sweep is initiated with pushbutton [15].

It is assumed that the upper and lower sweep limits are set and that, for example, the lower sweep limit has been reached. When the start pushbutton [15] is depressed a "1" is available at the output of the start flip-flop IC 2523/2.1 and the output of IC 2523/2.2 is set "O". Further setting is not necessary in this operating mode. When the start pushbutton is released a O-signal appears at the output of the start flip-flop. The release transistors T 2503 to T 2506 conduct during this period which means that O-signals appear at the outputs of IC 2527/4.1/2/3/4. The output of the direction flip-flop has a "O" on pin 6 and a "1" on pin 8.

When the start pushbutton [15] was depressed the flip-flop IC 2529 in the selection logic I and the limit flip-flop IC 2518 was set at the same time. A"O" signal is present at the output of IC 2529/2.2 and IC 2528. This means that the release transistors T 2503/T 2504 for the upper and lower sweep limit are conducting (regulation circuit off). The release transistors T 2505/ T 2506 for the Ref.Freq. and MF also conduct under the control of the selection logic I. As the output of the limit flip-flop IC 2528/ 3.2/3 has "O" signal the direction flip-flop IC 2525 pin 6 has "O" signal and

10. DESCRIPTION OF FUNCTION

...in 8 has "1" gate IC 2531/2.2 for the ...per sweep limit is cut off i.e. T 2510 ... also cut off. The pulses coming from the sweep pulse generation circuits now pass through gate IC 2531/2.1 and cause T 2511 to alternately conduct and cut off. The pulses are integrated with C 2508. The frequency runs up to the upper sweep limit USL (see logic plan III, Section 7.2.2.4). When the upper sweep limit is reached then the DC potential, dropping from a more positive voltage, crosses the reference voltage at the positive input of the comparator IC 2506 and the output steps to +12 V. This causes the minus input of the Schmitt IC 2504 to become +12 V and the output steps to -12 V.

The potential is reduced to -5 V via the divider R 2515/R 2516. This 1-signal is now passed to the input of IC 2524/6.1. From here the selection logic II switches on the regulation circuit for the upper sweep limit (T 2503 cut off) and the direction flip-flop IC 2525 has a "1" at pin 6 and "0" at pin 8. At the same time the logic circuit IC 2514/4.2/3 changes the state of the limit flip-flop IC 2528/3.2/3 and its output now has a "1". This means that gate IC 2531/2.1/2.2 is cut off. The upper sweep limit is thus reached, the regu...tion circuit for the upper sweep limit ...activated, and the sweep operation is ...topped. The sweep operation is initiated again only when pushbutton 15 is depressed again. The sweep operation now runs from the upper sweep limit to the lower sweep limit.

10.2.1.4.2. Continuous Sweep

In continuous sweep mode the sweep operation runs continuously from one sweep limit to the other.
This is implemented by deactivating the limit flip-flop IC 2528 i.e. a "0" signal is present at its output. The reversal of the sweep direction when a sweep limit is reached is controlled by the direction flip-flop IC 2525. In addition the release transistors (regulation circuit switches) T 2503 to T 2506 conduct during the whole sweep operation (regulation circuit inactive). This control is carried out by a 1-signal at the output of inverter IC 2524/6.4.

10.2.1.4.3. Rapid Sweep Adjustment

This circuit has the task of adjusting the measuring frequency, which may lie outside the sweep limits when sweep operation is started, rapidly to the ...ep limit and carrying out further ...ep with the sweep operations with the selected sweep rate. The MF is always pulled into the sweep limit which is closest to the MF. If the TF is outside the sweep limits then both Schmitt triggers IC 2504/IC 2505 have a "0" at the output. This means that the output of the NAND circuit IC 2514/4.2 and the output of the NAND circuit IC 2531/4.2 both have a "0". One or the other gate in IC 2531 is continuously opened with this 0-signal. This activates the rapid adjustment and causes one of the transistors T 2510 or T 2511 to conduct so that capacitor C 2508 can charge itself rapidly to the required voltage.

10.2.2. Modulation Frequency Generation (24)

The modulation frequency generation circuits have the task of generating the 41.6 Hz split frequency and the 166.6 Hz identification signal. As the identification frequency is used for modulation of the split frequency only in the last fifth of the reference cycle an auxiliary circuit is necessary.

In order to simplify the explanation of the various functions timing diagrams are available for the various functional sections. The signal designations refer directly to the specifications in the circuit diagram.

10.2.2.1. Generation and Signal Path of the Split Frequency

The 41.6 Hz split frequency is generated in a sine-wave oscillator. This oscillator consists of the double transistor T 2401 which is fed by a constant current source T 2402. The resonant circuit is formed by capacitor C 2404/ 0.47 uF and the active inductance IC 2401/24 H. Feedback is provided via IC 2402, R 2412, and C 2406 to the base of T 2401/2. The frequency of the oscillator is adjusted with P 2401. The range of adjustment is $f_o \pm 0.83$ Hz. The modulation factor m = 40% for the whole test set is adjusted with potentiometer P 2402. The voltage at TP 2401 after this adjustment is $V_{pp} \approx 10$ V. Range of adjustment: $V_{pp} = 10\ V \pm 15\%$.

At the point where the test set switches from the reference cycle to the measuring cycle it is necessary that the split frequency signal has a phase relationship which complies with the CCITT Regulations (see Timing Diagram for Generator). For this reason the split frequency signal is additionally shifted by 90° . In order to prevent loading of the resonant circuit the split frequency is extracted via the impedance converter stage IC 2402 and divided between two

paths. The first path leads to the test circuit and the second via the 83.6° phase shifter to the adder IC 2404.

The phase can be adjusted within a range of ±0.6% with the aid of potentiometer P 2403.

In the adder the phase of the split frequency is shifted by a further 6.4° so that the total phase shift is 90°.

10.2.2.2. Identification Frequency Generation

Two 41.6 Hz square-wave signals, with a phase relationship of 90°, are required for generation of the identification frequency. One signal is extracted at the collector of T 2401/2 and the other at the output of IC 2403. The signal extracted at the collector of T 2401/2 is fed through the transistor stages T 2403/2404/T2414 and IC 2407/6.1 and shaped into a square-wave signal.

The signal coming from IC 2403 with a phase shift of 83.6° passes through a further phase shifter of 6.4° and thus receives the necessary 90° phase shift with respect to the 41.6 Hz signal at TP 2401.

The signal fed through transistors T 2410/1/2 and T 2411 is shaped to a square-wave. The square-waves present at point a and point b have a phase relationship of 90°. Both square-wave signals are passed through the appropriate differentiation circuits C 2417/ R 2457 and C 2418/R 2460 and via the directional diodes GL 2406 to GL 2409 to the 3 ms single shot T 2413/T 2414. The identification frequency is generated in this single shot and extracted at the emitter of T 2415. The idle time of the the 3 ms single shot is adjusted with P 2406, see timing diagram of generator (24) TP 2403.

10.2.2.3. Identification Signal and Identification Pulse Generation

The task of the identification generation circuits is to control the 166.6 Hz identification frequency with auxiliary signals in such a manner that the identification frequency appears only during 24 ms at the end of the reference time.In order to achieve this the 41.6 Hz square-wave signal is extracted at the collector of T 2412 and passed via a second path, namely via inverters IC 2407/6.2, to the divider stage IC 2406 where it is divided in the ratios 5:1 and 10:1. The identification signal (E) is generated by logical combination of these two signals with the identification frequency in IC 2408 (See timing diagram generator (24) TP 2403).

A further logical combination of the divided signals in IC 2407/6.4 is used to generate the identification pulse (F) ; see generator timing diagram.

Before the identification signal (E) can be added to the 41.6 Hz split frequency (H) however it must be free of any DC component i.e. it must be converted into a symmetrical alternating voltage. This is done in the identification signal insertion circuit T 2406/T 2407. The identification pulse (F) is required for this operation. The removal of the DC component from the identification signal is necessary so that there is no DC potential at the output of the adder. The identification signal available at the output of the insertion circuit at point c is fed to the input of the adder IC 2404 together with the edge frequency, where these two signals are added together. The added signal is available at TP 2402 (see generator timing diagram). The voltage after adjustment of the modulation factor is V_{pp} = 4 V. As the inverting input of the adder represents a fixed zero no signal can be measured at this point. The signal is fed in as an input current.

In addition to addition of the split frequency to the identification signal the adder also reduces the steepness of the leading edge of the identification signal to approximately 640 µs (CCITT recommendation). The reduction is carried out by the R-C circuit R 2444/ C 2411. As this R-C circuit also results in a phase shift of the split frequency by 6.4° the phase shift in the phase shifter circuit could not be made 90° but had to be reduced to 83.6°.

10.2.2.4. 100 ms Gate Time Generation

The 100 ms gate time is the time base of the frequency counter and thus determines the accuracy of the frequency display in the LD-30.

A 4 ms single shot IC 2410 is required for generation of the gate time and is started with the positive going edge of the 5:1 divided signal. The output signal of the single shot is combined logically in a NAND-Circuit IC 2408/3.2. Further logical combinations with the 4.16 Hz "b" signal in the NAND-circuit IC 2408/3.3 are used to generate the 100 ms gate time. The gate time is adjusted to 100 ms with P 2407.

10. DESCRIPTION OF FUNCTION

As the NAND-circuit IC 2408/3.2 is driven by input signals with the same source (IC 2406/14) but with differing delays interference pulses which cause errors in the frequency display are generated at the output of the NAND-circuit. In order to avoid this the input signal at pin 2 of IC 2408/3.2 is fed via T 2416 and the delay circuit R 2480/C 2424 to a third input (pin 13) of the NAND-circuit (see Figure 10-4).

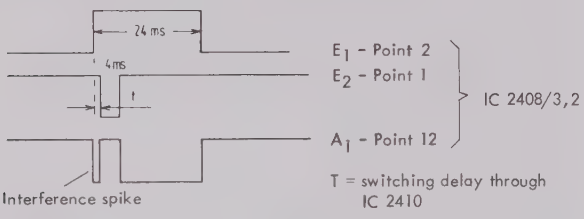


Figure 10-4a

The interference pulse is avoided by delaying the input signal E_1 with RC-circuit R 2480/C 2424 (see Figure 10-4b).

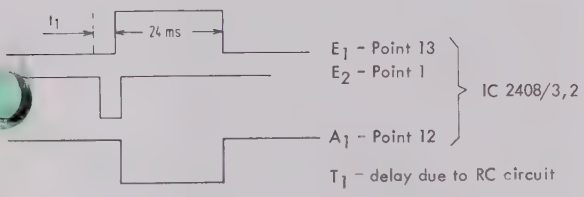


Figure 10-4b

10.2.2.5. Test Circuit

The test circuit has the task of generating an attenuation step of 1dB and a delay of 1 ms for a functional check of the test set LD-30.

When pushbutton [6] is depressed the 4.16 Hz "a" signal present at diode GL 2402 becomes active and switches T 2405 on and off. This causes a DC current to be alternately switched on and off from the -12 V line via R 2433 and R 2434 to the input of the adder which results in the same voltage step at the output of this circuit. By means of suitable amplification in the modulator (23) and the following amplifier chain the 1 dB level step is then generated and is available at the output of the generator.

The split frequency at TP 2401 and the split frequency shifted by 83.6° at point (H) are fed via suitable resistor arrangements to the test circuit (R 2432 R 2434 R 2433 and R 2428) for generation of the 1 ms delay.

Using the same 4.16 Hz timing pulse as for the attenuation step, either the split frequency from TP 2401 is fed via the resistor arrangement or the split frequency from point (H) is fed via R 2428 to the adder IC 2404. The resistor combination used results in a phase shift of the split frequency between the reference and measuring cycle of $15^{\circ} \cong 1$ ms.

This 1 ms is available at the output of the generator for a test of the LD-30 test set.

10.2.3. Modulator and Output Amplifier (23)

The carrier signal 200 Hz to 20 kHz is modulated with the split and identification frequencies (41.66 Hz and 166.6 Hz) in this assembly. The output amplifier amplifies the signal from the modulator to the necessary power.

10.2.3.1. Modulator

The modulator operates on the principle of current distribution control in the differential amplifier T 2304.

The carrier voltage is fed to the differential amplifier T 2304 via the output divider R 2317/R 2328. The output level of the generator is set to its required value with potentiometer P 2303. The coupling capacitor C 2304 provides DC insulation between the modulator input and the sine-wave shaper.

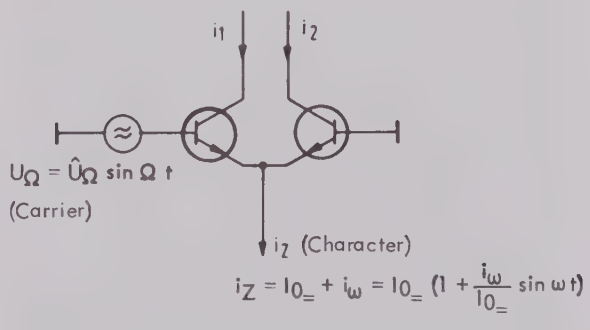


Figure 10-5

The 41.6 Hz modulation signal (split frequency) is fed to the amplifier IC 2302 via GL 2301/R 2306 and GL 2302/R 2307. This amplifier controls the differential amplifier stage T 2305. In this differential amplifier stage the

10. DESCRIPTION OF FUNCTION

41.6 Hz modulation frequency is overlaid on the emitter current of T 2304. Alignment of the modulation distortion for k_2 is carried out with potentiometer P 2302 by equalization of the collector currents of T 2305/2.1 and T 2305/2.2 via amplifier IC 2302.

The relationship between the peak value of the modulation signal and the emitter DC current I_o determines the modulation factor "m". The amplitude modulated carrier signal is available as an antiphase signal on the two outer resistors R 2331/R 2332. The antiphase signal is amplified in differential amplifier and converted into a single phase signal. The differential amplifier has a feedback circuit via resistor R 2335 in order to obtain amplification of

$$V = \frac{R\ 2335}{R\ 2331} = 5$$

Resistor R 2327 ensures that the symmetry in the external circuit of the modulator T 2304 is not effected by feedback. The symmetry of the modulator is adjusted with potentiometer P 2304.

The effects of the dividers R 2331/ R 2335 and R 2332/R 2327 on the symmetry when the collector current varies are reduced by keeping the collector voltage constant. This is achieved with a second regulation circuit via the operational amplifier IC 2301 and the emitter-follower stage T 2303.

In order to obtain the maximum possible suppression of the 41.6 Hz modulation signal the differential amplifier IC 2303 must have a good in-phase suppression characteristic. This requirement is achieved by means of a regulation circuit. As soon as the collector currents of T 2304/2.1 and T 2304/2.2 have different values the differential amplifier IC 2303 is activated and a DC voltage appears at its output, is amplified via IC 2306 and IC 2305, and fedback to the base of T 2304/2.2. The collector current deviation is thus equalized and a high degree of modulator symmetry achieved. In order to avoid a delay, the modulated carrier signal must not be fedback to the base of T 2304/2.2. For this reason the feedback circuit is in the form of a low-pass filter. This consists of the integrator IC 2306 and an active low-pass filter with the operational amplifier IC 2305.

In the case of remote level control the emitter current of T 2304 is varied (m = constant) for continuous adjustment of the amplification. If the symmetry of the modulator is not to be disturbed by this adjustment the offset voltage at the input of the differential amplifier IC 2303 must be as small as possible. The offsets of IC 2303 and IC 2306 can be adjusted with potentiometers P 2305 and P 2308 respectively.

The value of the emitter current I_o for T 2304 is determined by the level of 60 dB during retransmission (remodulation). The lower current limit is determined by the residual currents and the upper current limit by the effect of the bulk resistances of the transistors T 2304/2.1 and T 2304/2.2. This results in a current range of I_o = 4 µA to 4 mA.

For emitter currents above 1 mA the emitter bulk resistances result in a noticeable current feedback. This means that an increase in the emitter current no longer corresponds to a linear change of the output level. For this reason a collector current is added via T 2301 whenever the control current $I_o > 0.8$ mA.

As a voltage which is proportional to the control current I_o is available at the output of IC 2301 this voltage is used for control of the current source T 2301. The collector current must not contain the carrier frequency as a carrier distortion factor k_2 would otherwise be generated in the modulator. C 2302 filters out the carrier voltage at the output of IC 2301. The voltage divider R 2304/R 2305 determines the starting point of the correction current.

In order to keep the modulation factor constant when the current I_o is varied the maximum current must not exceed 1 mA (current feedback due to emitter bulk resistances).

However as the modulator requires a control current of 4 mA the differential amplifier T 2305 must be followed by a current amplification stage. This stage is implemented with the operational amplifier IC 2304 with a current amplification factor of $V \approx 8$. The amplified current is fed to the modulator via GL 2308. In order to avoid a level dependent error in the current amplification the offsets of IC 2304 and IC 2306 must be aligned with the potentiometers P 2305 and P 2308 respectively.

In the case of retransmission (remodulation) the internal control current source is disconnected by means of switch T 2309 (GL 2308 cuts off). The external

10. DESCRIPTION OF FUNCTION

ntrol current is supplied by the eiver and fed into the modulator via 2303.

When retransmission (remodulation) is activated ($I_{remod.} > 0.5$ µA) transistor T2311 is cut off and T2312,T2313 conduct. T 2303 conducts again, the current amplification stage IC 2304 no longer being driven. A 1-signal for control of the carrier frequency switching is available at the collector of T 2313.

10.2.3.2. Remote Level Control

In the case of remote level control the current source T 2308 is replaced by a current source in the receiver of the LD-30. If the operating mode switch 22 is set to the position "Remote Control" transistor T 2203 is cutoff. In the other operating modes the control current from the receiver section is short circuited.

If transistor T 2203 cuts off transistor T 2306 is also cutoff by the control current. At the same time transistor T 2307 conducts and cuts off diode GL 2309. The internal current source is now disconnected. The differential amplifier T 2305 is fed from the external current source via diode 2307.

10.2.3.3. Output Amplifier,Level Attenuator, and Output Circuit

The level attenuator consists of a coarse attenuator and a fine attenuator. The coarse attenuator is a resistance attenuator with a high accuracy. It attenuates the output signal from the modulator IC 2303 in 5 dB steps in a range from -45 to +10 dBm.

The fine attenuator consists of the precision potentiometer P 2310. This has a knob with calibration marks and can be varied in the range from -6 to +1 dBm.

The output stage consists of an amplifier IC 2307. In order to obtain the required output power this stage is followed by a power stage consisting of T 2316 and T 2317.

The output transformer is connected directly. As feedback is carried out from the output of the power output stage the drift and offset of the output voltage is low so that the DC current through the primary winding remains sufficiently small. The main inductance of the output transformer Ü 2301 is large so that the load on the amplifier due to magnetization currents in the transformer at low frequencies remains as low as possible.

As the main inductance depends on the level i.e. it becomes smaller as the level is reduced, this would result in an unpermissibly large delay time at low frequencies and low levels. The feedback circuit consists of winding (1) / (2) , C 2335, R 23103, and R 2392 and is connected to the input of the operational amplifier IC 2307. This reduces the copper resistance of the primary winding by the feedback factor and results in a short delay time.

The feedback for high frequencies is via C 2334/R 2392, and the DC feedback via R 2395/R 2392.

In the case of retransmission (remodulation) T 2314 conducts and increases the amplification of the output stage by 10 dB. The output transformer converts the output signal by 3.5 dB. In the case of measurement in a closed communication loop the output transformer must carry part of the source current. An air gap prevents the transformer from being saturated by this. The secondary side of the transformer is symmetrical and is not grounded. The resistors R 23106/ R 23107, together with the copper resistance of the winding, result in an internal resistance of 600 Ohms. The units can be converted to an additional internal resistance.

10.2.3.3.1. Protective Circuit

When test connections are established between the output of the LD-30 and the transmission lines high voltage peaks can occur which can then reach the amplifier output via the output transformer and can cause destruction of transistors T 2316/T 2317. This is avoided by T 2315 which is normally cutoff. If positive voltage peaks occur at the emitter of T 2316 then this transistor would be overloaded if T 2315 were not fitted. The fact that T 2315 is there results in this transistor conducting and preventing T 2316 from being destroyed. In the case of negative spikes T 2316 continues to conduct.

10.2.3.4. Coupling Stage for Telephony

Using the speech equipment of the test set LD-30 it is possible to establish a telephone connection via the test line to the opposite end of the line. When the test connection exists the speech is

passed from the wire to the generator output socket Bu 2301 via the transformer Ü 2301 and to the output amplifier stage (emitter of T 2316).

This point is kept at a voltage of 0 and a current change is thus forced in T 2316, this current being split at the collector via C 2336 and C 2344. The part of the collector current which flows through C 2344 drives IC 2308 whose amplification is in the order of V ≈ 560. The speech signal amplification between the speech signal input (output Bu 2301) and the output (23) 17 is approximately 0 dB. In order to deactivate the generator signal at the telephone output the generator signal from the output of IC 2307 is fed via potentiometer P 2313 and R 23117 and R 23112 to the input of IC 2308, the generator signal being cancelled at the junction of R 2311 due to the reversed phase.

Alignment of the internal sound suppression is carried out with potentiometer P 2313.

10.2.4. Frequency Counter (26)

The frequency counter consists of a frequency multiplier (10 x) and the actual counter with the following display control. The multiplier receives the saw-tooth signal of the carrier frequency switching. This signal is fed to the inputs of the comparators IC 2619 to IC 2622. The non-inverting inputs are connected to reference dividers which determine the switching thresholds in accordance with the timing diagram (Figure 10-6) for the saw-tooth signal.

As the saw-tooth wave form rises or falls the reference points of the various comparators is passed sequentially and the outputs step sequentially to "1" or "0" respectively. By means of suitable logical combinations of the output signal from the comparators using exclusive-OR circuits in IC 2618 a square-wave signal with 5 x the input frequency is available at output 8 of IC 2618/4.1.

The multiplied MF at the output of the Schmitt trigger IC 2617/2.1 (TP 2601) is fed to the counter input IC 2613/4.4. The time base (100 ms gate time) is fed to the second input of this stage. This means that the frequency counter counts only for 100 ms during the measuring cycle. The resolution of the measured frequency if 1 Hz. As this resolution is not normally required however a frequency divider IC 2615 follows the output of IC 2613/4.4 and divides the multiplied frequency in the ratio 10:1 (resolution 10 Hz). This is the case when pushbutton [7] is not depressed. If pushbutton [7] is depressed the resolution is 1 Hz as the 10:1 divider IC 2615 is deactivated. This control is logically provided by the AND-OR gate IC 2614.

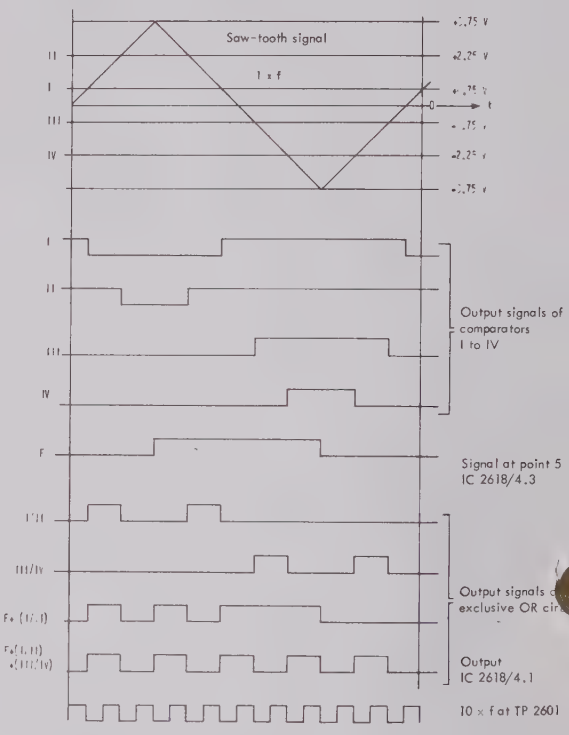


Figure 10-6

At the end of the gate time the counting operation is interrupted and the store pulse generated simultaneously with single shot IC 2616. This instruction causes the counter value of IC's 2601 to 2604 to be transferred to the buffer IC's 2605 to 2608 and stored. The trailing edge of the store pulse is differentiated by means of C 2601/R2632 and is used for resetting the counter.

The driver stages IC 2609 to 2612 convert the BCD code into 7 segment display code and permit the display of the counter value via the display units IC 2601 to 2604.

The display is implemented with large size Minitron units.

Switch [8] can be used to switch the display between the generator and receiver frequencies.

10. DESCRIPTION OF FUNCTION

The multiplied (10 x) generator or receiver frequency is passed via IC 541/ 2.2 to the frequency counter.

10.3. DETAILED DESCRIPTION OF RECEIVER ASSEMBLIES

10.3.1. Input Amplifier (2)

10.3.1.1. Input Circuit

The signal applied to socket 301 is fed through the operating mode switch and the Ri field to the symmetrical floating input transformer Ü 201. The transformer Ü 201 is included in the feedback loop of the input amplifier. This means that the internal resistance of the transformer is so low that the input resistance of the receiver is formed mainly by the resistors R 201 and R 202.

The complete amplifier consists of two identical amplifiers which are joined together again in the demodulator (T 211 to T 214).

A high pass filter with f_g = 16 Hz is fitted directly at the input. This high pass filter is intended to suppress interference due to dialling noises. The high pass filter does however cause a delay error at 200 Hz.

The low limit frequency requires a very large value for C 203 or C 204 (≈ 1050 µF). A reduction can be achieved by tapping off a partial voltage on the capacitor. The effective capacitance is increased in accordance with the dividing ratio. The voltage on the capacitor is picked up with T 201, T 202 and the divider is formed by R 213, R 214 and R 215 R 216 respectively.

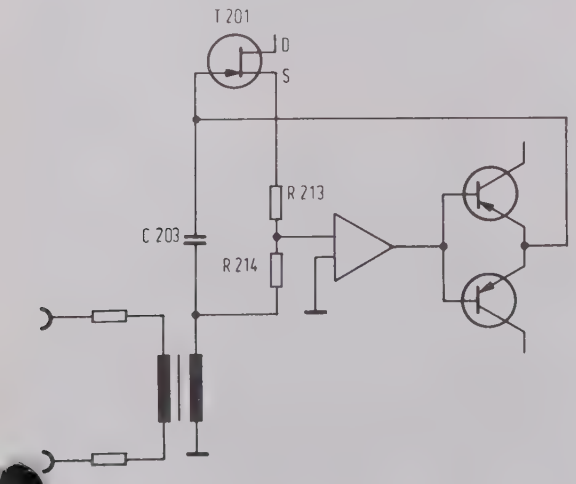


Figure 10-7

The amplifier is divided into two feedback loops in order to attain better stability.

Loop I : T 201-T 205-T 207-T 211-T 201
Loop II: T 201-R 213/214-IC 201-T 203-T 207-T 211-T 201

The overall loop amplification is 96 dB and is divided approximately equally between the two loops. The complete amplifier has a feedback which results in an amplification of one together with the demodulator and has a relatively wide bandwidth

The components L 203, R 232 and R 233, C 215 and R 236, and C 217 are used for stabilization of the feedback at high frequencies.

The transistors T 208 and T 209 form the load resistors of T 207 and T 210 respectively. These are connected as current sources in order to attain a high amplification and in order to supply sufficient current for reverse charging of C 217, C 218. T 207 and T 210 are controlled by IC 210 which is followed by the common-collector circuits T 203, T 204 in order to reduce its output resistance.

T 205, T 206 are used as isolating stages.
A partial current for the frequency counter is extracted via Ü 202. The diodes GL 211 to 214 and GL 223, GL 224 prevent the operational amplifier from drifting into a limiting state if the supply voltages are connected with a time difference.

10.3.1.2. Demodulator

A current source is required for supplying the logarithmer and for this reason the working current is extracted from the collector of a transistor (T 211,214). The fact that the collectors are connected together results in a two-way average value rectifier. The frequency doubling effect simplifies filtering of the remaining carrier in the carrier frequency filter circuit which follows.

The following relationship exists between the input voltage (Bu 201) and the rectified output current:

$$I = \frac{V.\sqrt{2} \cdot 2}{600 \cdot \pi}$$

V: RMS value of the input voltage
I: DC output current from the

demodulator

The resulting currents are for
+10 dB: 3.0 mA
-50 dB: 3.0 µA

Rectification is actually carried out in the emitter of transistors T 211, T 214, the unused half-cycle being drained via T 212 and T 213 respectively. Transistors T 211 and T 214 must have high current amplification factors so that a minimum amount of working current is lost through the base. Transistors suitable for this purpose have high base - emitter capacitances which again means current losses at low levels. The unwanted capacitances are neutralized by "rapid" diodes (GL 207 to 210) connected in series with the emitter. The diode threshold voltages are compensated partially by GL 204 and GL 205. The frequency response of the output current for a constant input voltage is
200 Hz to 20 kHz: ≦ ± 0.05 dB
with reference to 1.8 kHz

10.3.1.3. Carrier Frequency Filter

The demodulated signal contains residual carrier signals with double frequency. These must be attenuated in order to prevent them causing DC shifts in the logarithmer. For this purpose the signal is passed through the carrier frequency filter. The following attenuation values are implemented:

Attenuation Δ a at 200 Hz: ≧ 4 dB
Attenuation Δ a at 400 Hz: ≧ 17 dB
Attenuation Δ a at ≧ 800 Hz: ≧ 39 dB

The carrier frequency filter is an active filter with one peak at 800 Hz (IC 203) and a second order low pass filter (IC 204).

The filter is driven from a high impedance source and terminated with a low impedance.

Resistor R 259 is used to flatten the peak and also to decouple from the following low pass filter.

The low pass filter consists of the two RC circuits R 267/C 235 and R 262 + R 268/C 230 which are coupled together via the amplifier IC 204.

C 236 is used to stabilize the low pass filter as the input resistance of the logarithmer increases at higher frequencies.

10.3.1.4. Logarithmer, Retransmission (Remodulation), Remote Level Control

The input signal (current from the demodulator) is logarithmized and converted into a voltage which now has a linear relationship to the input level (in dB). This means that the meter scales for level and attenuation are linear. The split frequency which is overlaid on the input signal appears at the output with a voltage which is independent of the input level. The voltage remains constant as the split frequency signal is now logically combined with the carrier level by means of the modulation factor.

The base - emitter diode of transistor T 218/2.2 is used to logarithmize the signal. With an impressed current the voltage follows the general function for diodes.

$$V = V_T \ln \frac{I}{I_o}$$

V_T is temperature dependent which means that a temperature dependent sensitivity error is generated, this error being compensated in the following amplifier by the temperature dependent resistor R_{Cu} .

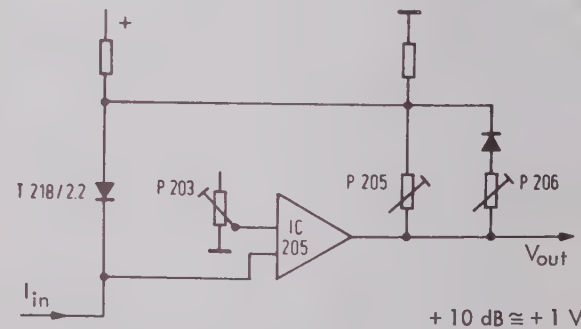


Figure 10-8 Basic circuit diagram Logarithmer

As the logarithmer represents the termination resistance for the carrier frequency filter the input resistance must be low in comparison to the termination resistor (R 268) to prevent it having an effect in the case of level changes (delay error). This is achieved by including the logarithmer diode in the feedback loop of the following amplifier. With the existing high loop amplification (T 219 approx. 20 dB,

10. DESCRIPTION OF FUNCTION

205 approx 80 dB) the dynamic resistance of the diode becomes so small that it can be neglected.

In order to attain the output voltage of 1 V/10 dB which is needed for the following circuits the feedback of the amplifier is adjusted so that the amplification is 33.4. This amplification can be adjusted with potentiometer P 205. Potentiometer P 203 is used for adjustment of the zero point (0 dB ≅ 0 V). The other half of the transistor (T 218.2.1) is used for drift compensation of the logarithmer diode; this half of the transistor is operated with an impressed current and is connected to the inverting input of IC 205 via T 219/2.1.

A heating effect occurs in the logarithmer diode even due to the split frequency itself. At large levels the heating of the crystal varies in the rhythm of the split frequency. This means that the diode behaves as if an inductance were connected in series with it, the value of the inductance being dependent on the input level. This behaviour results in an attenuation dependent delay error.

This behaviour is compensated by coupling an antiphase voltage via Ü 203, 204, T 218/2.1. As this voltage is taken from the primary side of Ü 203 it is also phase shifted inductively with respect to the current.

Due to the logarithmer the overlaid split frequency signal provides a DC component corresponding to approximately 0.3 dB. If alignment is carried out with a modulated input signal this error occurs whenever level measurements are carried out with unmodulated signals. The zero point correction is used to correct this error. The error is compensated by an additional current via resistor R 296 and GL 222.

With a modulated signal, -12 V is available at pin (2) 12 (GL 222 cut off); when the signal is not modulated pin 12 has a high impedance and the additional current flow is via R 296 and GL 222 (see also description of identification channel (4) Section 10.3.2.2).

If the retransmission (remod.) connection is established with the operating mode switch [22] T217 is cut off by a DC voltage coming from the generator. The DC current with the overlaid split frequency and identification signals

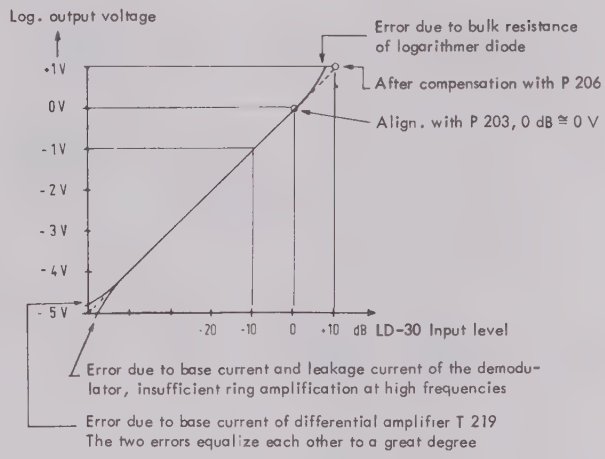

Log. output voltage
+1V
0V
-1V
-2V
-3V
-4V
-5V
-20
-10
0
+10
dB LD-30 Input level
Error due to bulk resistance of logarithmer diode
After compensation with P 206
Align. with P 203, 0 dB ≅ 0 V
Error due to base current and leakage current of the demodulator, insufficient ring amplification at high frequencies
Error due to base current of differential amplifier T 219
The two errors equalize each other to a great degree

Figure 10-9 Signal behaviour of the output voltage of the logarithmer

coming from the demodulator now flows to the generator and modulates this unit.

The current is not logarithmized

+10 dB = 3.0 mA
-50 dB = 3.0 µA

The functions of the LD-30 remain active and remote level control is disconnected.

The indication errors are slightly larger due to the increased collector voltage on T 218/2.2

Remote control of the generator level is possible within the range +1 to -40 dB. For this purpose a voltage proportional to the input voltage (not logarithmized) is tapped off at R 277 and is processed further in the "buffer for remote level control" (11) (option).

If the level 0 dB is exceeded T 215 takes over the current to prevent T 217 from being saturated.

A current proportional to the input level is supplied at the output of the buffer for remote level control (Bu 102)

+1.0 dB ≅ 1 mA
-40 dB ≅ 8.91 µA

10.3.2. Evaluation Circuit (4)

The evaluation circuit separates the functions.

Delay measurement, level and attenuation measurement, and generation of the set pulse from the identification signal.

10. DESCRIPTION OF FUNCTION

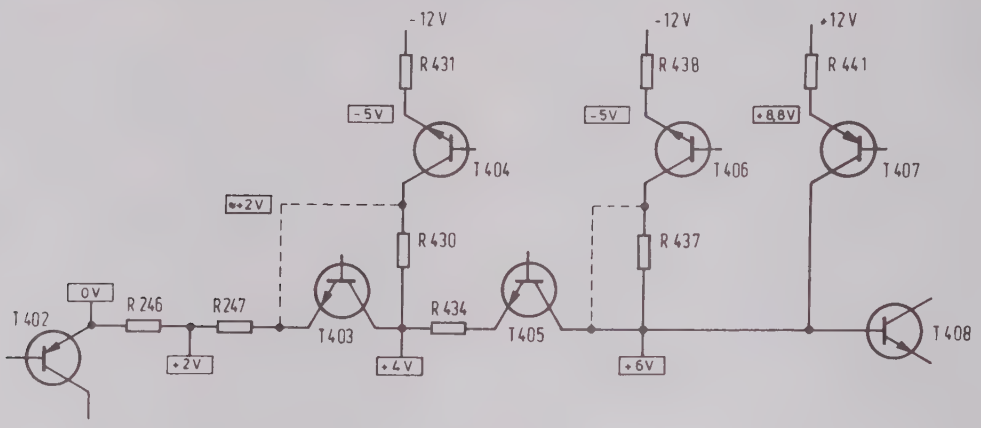


Figure 10-10 DC Potentials in the residual filter

10.3.2.1. Split Frequency Filter

The split frequency (f = 41.6 Hz, V_{pp} = 700 mV) with the information of the phase shift is available at the input of the split frequency filter. The zero transitions of the split frequency are evaluated in order to determine the phase shift for display of the group delay time. Interference on the split frequency is very bad as it shifts the zero transition. A high quality active filter was used so that the split frequency filter can fulfil the requirements.

The components C 401, 402, R 401, 402 represent the double element high pass filter with f_g = 15 Hz.

The following amplifier (V ≈ 20) with its feedback represents a low pass filter with f_g = 100 Hz. It also has the task of limiting the large interference peaks when the attenuation is switched. The following divider 10:1 (R 405, R 406) reduces the working signal amplitude to V_{pp} = 0.6 V.

This is followed by an acceptor circuit (f_r = 125 Hz) with C 407 and the active inductance C 406, IC 402. The resonant frequency is adjusted with potentiometer P 401. The isolating stage T 401 is followed by a second acceptor circuit (C 412, IC 403) which is aligned to f_r = 83.3 Hz. The following residual filter has peaks at 360 Hz (C 419, C 420, IC 404) and 200 Hz (C 426, IC 405).

The filter should be fed with R_i = 0 and with an infinite output resistance. The transistor T 402 is operated with an emitter current of approximately 0.6 mA as is T 401 for distortion and noise reasons. This current is generated in the current source T 407 and flows through the residual filter in order to provide the required working point for the operational amplifiers for the inductances.

The isolation stage T 408 is again followed by a high pass filter C 431, R 450, C 432, R 451 for DC decoupling of the zero transition detector IC 406. In this detector the split frequency sine-wave is converted into a square-wave voltage with a very steep edge (fall-of time ≦ 10 ms/5 V). The offset adjustment of IC 406 is adjusted with potentiometer P 403.

With very low input signals (-65 dB) or with the input open the split frequency and identification channel should be "killed" in order to avoid incorrect synchronization. The pointer of the meter oscillates from one end of the scale to the other. For this purpose transistor T 410 is cutoff by a negative voltage (-6 to -8 V) from the amplitude channel, T 409 conducts, and IC 406 switches its output to approximately +5 V.

At the same time the identification pulse is shorted to ground via GL 409 and T 409. If the receiver is operated with an unmodulated signal (used as a level meter) T 409 also conducts due to a positive voltage from IC 419. The decisive factor for missing modulation is the fact that the identification signal is not present.

After removal of the split frequency the timing pulses continue to be supplied by the multivibrator T 415 to T 417 which now runs freely. This means that the unit remains functional for level measurements.

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10.3.2.2. Identification Channel

At the end of the reference cycle the generator transmits an identification signal f = 166.6 Hz, t = 24 ms in order to synchronize the receiver. This signal is filtered out and used for generation of identification pulses. In order to prevent generation of false pulses if interference voltages are received from the test line a working-interference rectifier circuit was used. If large interference voltages occur for a short time the identification pulse generation is inhibited. The receiver has to synchronize itself during this period. If the interference signals happen to have the same frequency as the identification signal false pulses cannot be avoided

Two RC circuits R 497/C 445 and R 499/C 448 which have a pass range of 20 Hz to 400 Hz are fitted at the input of the identification channel. IC 413 has an amplification factor of V ≈ 45. The identification signal must not be limited at this point; only large interference spikes which occur when the attenuation is switched must be limited. The divider R 4100/4101 feeds the filter with a peak at f = 166.6 Hz which is constructed with an active inductance 449, IC 415.

The working signal channel receives its signal from the output at IC 415. The signal is passed through a full-wave rectifier GL 407/408, the amplifier IC 417 with V = -1 being connected in the negative path. The output of the working signal is connected to the negative inputs of the comparators IC 418 and IC 419.

The interference signal at TP 405 consists of interference frequencies which come from the test line, the harmonic k_2, the split frequency f = 83.3 Hz (distortion factor of the logarithmer) and remains of the identification signal.

Amplifier IC 414 is followed, in a similar manner to the working signal channel, by a full-wave rectifier which is however designed as a peak rectifier with a discharging time constant of approximately 25 ms. This means that the output is the envelope curve rather than the separate half waves of the identification signal. Comparator IC 418 compares the decaying interference signal rectifier voltage (envelope curve) and the increasing working signal rectifier voltage (half-waves).

The amplification is adjusted with potentiometer P 404 so that the sixth half-wave of the working signal rectifier generates the first identification pulse.

This first impulse is decisive for synchronization of the receiver. Correct synchronization is also guaranteed if the first identification pulse is initiated by the fourth to eighth half-wave of the working signal rectifier.

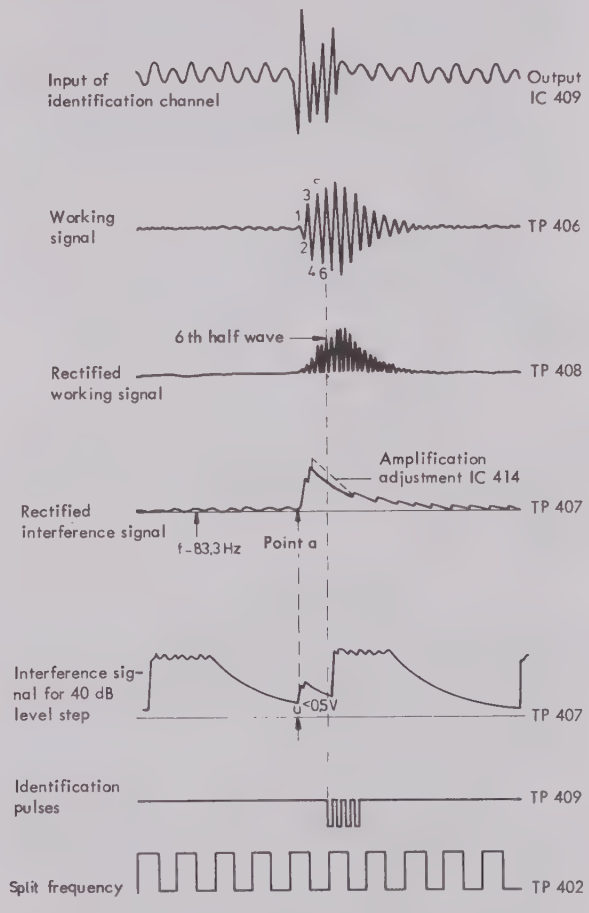

Figure 10-11 Signal and pulse diagram in the identification channel

If large interference signals are present then the interference signal rectifier voltage increases but the operating time of the comparator is shifted from the sixth to the seventh eighth or ninth half-wave. If the shift is to the ninth half-wave or further capacitor C 453 is charged to such a degree that no further identification pulse is generated. IC 413 is used for limiting the interference spikes

This means that the charging voltage for C 453 is limited. The time constant of C 453/R 4115 is selected so that the DC voltage drops to a normal value before the identification signal arrives (see Figure 10-11 pulse diagram, identification channel, TP 407).

Comparator IC 419 uses the working signal rectifier voltage to determine whether an identification signal is present or not. If the identification signal is present a DC voltage of approximately +4 V is present at input 2 of IC 419 and the output is -12 V.

GL 413 is thus cutoff and GL 414 conducts. This means, for the logarithmer; modulation present (see description of logarithmer, Section 10.3.1.4.).

If the identification signal is missing input 2 of IC 419 drops to +1.5 V and the output switches to +12 V. GL 413 conducts, the split frequency filter output is "killed" via T 409, and the generation of further identification pulses is prevented via GL 409 (faulty pulses due to interference or noise).

The RC-circuit R 4210/C 454 prevents IC 419 from reacting during short term failures (≦ 5 s) of the identification signal. As long as the split frequency signal is present the test set remains fully functional during these 5 s.

10.3.2.3. Amplitude Channel

The signal coming from the logarithmer is freed of overlaid signals in the amplitude channel. This is necessary for processing in the indicating amplifier for level and attenuation measurements.

The signal contains a logarithmized DC voltage derived from the carrier level (measuring and reference frequency), overlaid split frequency, identification frequency, and residual carrier. Only the logarithmized DC voltage is required at the output for the level and attenuation measurement.

A high and low signal indicator (Gl 403, Gl 404) is provided to indicates when the measuring and reference frequencies are outside the permissible range of input level (-50 to +10 dBm).

The appropriate indicator should react when the signal is more than 2 dB outside the range.

The input of the amplitude channel (R446) is the same as the identification channel as far as the output of IC 409.

At this point the identification channel is tapped off via C 445.

The filter with a peak at 41.6 Hz is common to the amplitude and identification channels.

The remaining requirements for the amplitude channel are achieved by the active low-pass filter (IC 410) with a limit frequency of 13 Hz.

In addition to the attenuation requirements the amplitude channel must also settle rapidly when sudden level changes occur.

The comparators IC 411 and 412 are used for initiating the high and low signal indicators. These compare the current DC voltage in the amplitude channel with a fixed divider voltage (R 481/482 and R 483/484 respectively).

10.3.2.4. Time Base

The 198 ms single shot is started by the first identification pulse. After 198 ms the 22 ms pulse stage is started. An split frequency pulse from the multivibrator which arrives within this period of 22 ms generates the set pulse for FF1 and FF2 at pin ④ 10.

If the identification pulse is missing T 419 conducts and C 465 is discharged. If however an identification pulse is available at TP 409 T 419 is cutoff. C 465 begins to charge via R 4142.

When the voltage of the divider R 4143/ 4144 is reached the output of the comparator IC 421 switches to a

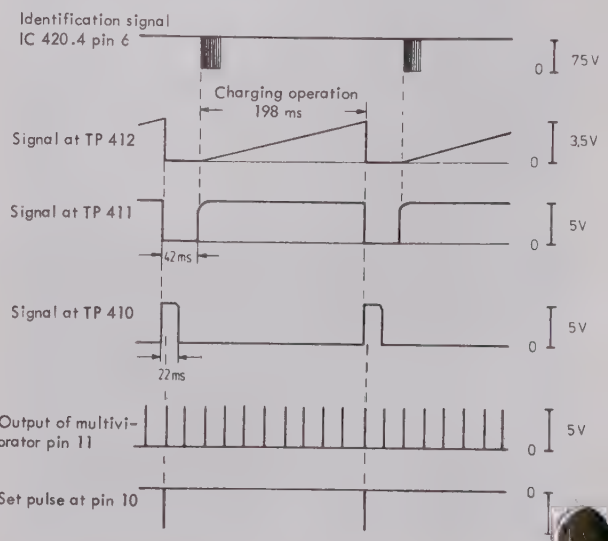

Figure 10-12 Pulse diagram of the time base

10. DESCRIPTION OF FUNCTION

gative potential; the charging eration is terminated via IC 420.3 nd IC 420.4 and C 465 is discharged again via transistor T 419.

Only when this has occurred can a further identification pulse start the charging operation again.

When the signal at TP 411 switches to O V the transistor T 418 is cutoff via C 461 and the potential at the output TP 410 switches to +5 V. Transistor T 418 remains cutoff until C 461 is charged in the opposite direction via R 4132 (22 ms ± 2 ms).

10.3.2.5. Multivibrator

The multivibrator is the internal timing pulse generator of the receiver. When the test set is used as a level meter the multivibrator runs freely. If a modulated generator signal is connected the multivibrator is synchronized via C 455 with the split frequency which is present in the form of a square-wave signal.

If an split frequency pulse arrives during the pulse time of the 22 ms pulse stage the AND circuit IC 420/4.2 supplies a set pulse which is used in e indication amplifier ③ for setting lip-flop 1 and FF 2, see pulse diagram in Figure 10-12.

The output pulses are passed from IC 420/4.1 with a delay (C 459) via pin ④ 11 as clock pulses to FF1 and FF 2.

For the following description it is assumed that the multivibrator is running freely and that there is no split frequency signal at capacitor C 455. T 417 is cutoff, T 415 is conducting and T 416 also conducts with an emitter voltage of -0.3 V via resistor R 4126. Capacitor C 457 is charged via resistor R 4127 until the threshold voltage of T 417 is reached. T 417 now conducts.

The negative pulse is passed via capacitor C 458 to transistor T 415 which is cutoff by the pulse. The base of transistor T 416 has a voltage of +5 V and the emitter 4.4 V. C 457 is charged via transistor T 416. T 417 continues to conduct until capacitor C 458 is charged in the opposite direction via R 4124 after 0.3 ms. After this transistor T 415 conducts and the emitter of T 416 is connected to -0.3 V.

The operation starts again when capacitor 457 is charged in the opposite rection via resistor R 4127 (see gure 10-13).

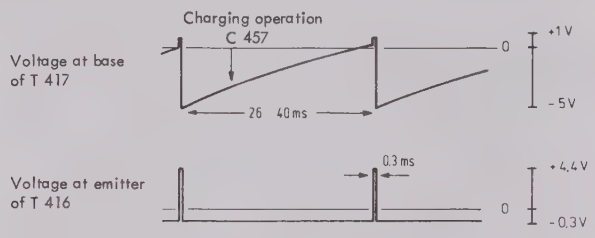

Figure 10-13 Pulse diagram for C 457

If the split frequency square-wave voltage arrives at the input of capacitor C 455 the negative edges of the signal initiate the 0.3 ms pulse. The charging operation of capacitor C 457 is terminated prematurely and this capacitor then operates purely as a coupling capacitor.

This means that the pulse frequency is equal to the split frequency. The pulse length (0.3 ms) is however still controlled by the RC circuit C 458/R 4124.

10.3.2.6. "100 ms" Single Shot, 4-9-14 ms Delay Circuit

The 100 ms single shot and the 4-9-14 ms delay circuit are the elements which determine the time for delay measurement. For this reason the circuits are designed for good short and long term stability.

After setting and the immediately following clock pulse FF 2 in the indication amplifier ③ is reset and supplies the signal "100 ms release" at pin ④ 7. The 100 ms single shot starts and supplies the start signal for the 9 ms delay circuit for delay time measurement after the 100 ms period has elapsed. After the total of 109 ms FF 2 receives its reset pulse via pin ④ 9 After the next clock pulse arrives FF 2 is again set and again provides the signal "100 ms release".

In position 1 of switch [11] (± 10 ms add +5 ms) the operating time of the delay circuit is changed so that it is 4 ms during the meas. cycle and 14 ms in the reference cycle. The difference of 10 ms results in a shift of the delay indication by 5 ms.

The positive signal component of the 100 ms release pulse charges capacitor C 473 when transistor T 423 is cutoff. When the divider voltage of R 4164, R 4165/4166 (≅ 100 ms) is reached the comparator IC 423 changes its output voltage from +4.6 V to -0.6 V. This is the starting point of the 4-9-14 ms delay circuit.

10. DESCRIPTION OF FUNCTION

If the switch [11] is set to one of the positions 2 to 9 transistors T 421 and T 422 remain cutoff. The 9 ms in the delay circuit are determined by the charging voltage of the RC circuit R 4153/C 470 and the divider voltage of R 4151/4152. The signal "reset FF 2" is available at the output of comparator IC 422.

Flip-flop 2 is now reset. The signal "100 ms release" has 0 V for discharging of the capacitors C470 and C 473. The 100 ms adjustment is carried out with potentiometer P 406 (see pulse diagram Figure 10-14).

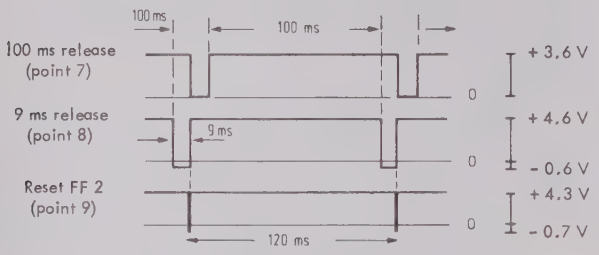

Figure 10-14 Pulse diagram for 0 ms delay

In position 1 of switch [11] signals synchronized with the meas. and reference cycles are connected to transistors T 421 and T 422 via pin ④ 5 and pin ④ 6

During the measuring cycle the transistor T 421 conducts and T 422 is cutoff. During the reference cycle the transistor states are reversed. This causes a reduction of the delay to 4 ms in the reference cycle by changing the divider voltage (+3.5 V) and a delay of 14 ms in the measuring cycle. P 405 is adjusted so that there is a difference of 10 ms between the delays of the measuring and reference cycles.

10.3.3. Indication Amplifier ③

10.3.3.1. Timing Pulse Generator

The timing pulse generates the necessary control signals for delay attenuation and level measurement from the signals offered by the evaluation circuit.

In order to simplify comprehension the 3 signals which are fed to the evaluation circuit are summarized here (see receiver pulse diagram in the appendix).

Set Pulse: Derived from identification signal; determines the assignment of the internal meas. and reference cycles to the generator signal.

Clock Pulse : Generated from the split frequency signal, pulse interval 24 ms; if there is a delay time the 24 ms pulse interval is changed at the point where the split frequency signal switches.

Reset FF 2: Pulse is generated by "100 ms release" and 9 ms delay circuit and resets FF 2.

The assignment of the internal cycles to the transmitted signal is carried out by setting FF1 and FF2. As all signals generated in the timing pulse generator are tied to the meas. and reference cycles the results of the test are displayed with the correct sign.

Flip-flop 2 (IC 303/2.1) is set by the clock pulse. The output of IC 303/2.1 at pin 12 has a "0" signal (100 ms release pulse) and pin 13 has a "1" . The JK inputs of IC 303/2.1 are reset after 109 ms but the flip-flop changes state only when the clock pulse arrives. IC 303/2.2 supplies the meas. and reference cycle pulses and IC 303/2.1 the 100 ms release pulse.

If there is a delay time on the test line the meas. and reference cycles have different lengths, starting from a length of 120 ms. In a similar manner the starting point of the 100 ms release is also shifted.

The time interval between the end of the 109 ms and the next start point of the 100 ms pulse is a dimension for the delay time.

10.3.3.2. Generation of the Output Signals

Comprehension of the following sections can be better understood if reference is made to the pulse diagram of the generator in the appendix.

10.3.3.2.1. Sensing TP 305

A sensing signal of 11 ms is generated at TP 305. For level measurements the sensing pulse is positioned within the reference cycle. With this pulse the result of level measurement of the received signal is transferred to the display buffer and displayed.

With pushbutton [32] depressed the sensing signal is shifted into the measuring cycle. In this case the reference signal is displayed.

10.3.3.2.2. Zero Sensing TP 306

The signal "Zero Sensing" is required in the indication amplifier only for level measurements. The zero point of the amplifier is obtained with the pulse "Zero Sensing" together with the pulse "clamp".

The conditions are fulfilled for a period of 11 ms if

Pushbutton [31] 5 is depressed, during the meas. or reference cycle according to position of pushbutton [32] .

Transistor T 303 conducts during this operation.

10.3.3.2.3. Clamp TP 302

The signal "clamp" is used for delay measurement to reset the test result (calibration of the phase meter).

For attenuation measurements the signal "clamp" is used to obtain the reference point in the reference cycle.

For level measurements the reference point is also obtain with this pulse together with the zero sensing signal. In this case it is a fixed voltage and depends on the selected measuring range.

For delay measurements the signal "clamp" is generated if the following conditions are fulfilled at IC 301:

During the measuring cycle, after the 1 ms release, end of 11 ms pulse from single shot IC 304/2.2, pushbutton [31] 3 depressed.

For attenuation and level measurements the signal "clamp" is generated if the following conditions are fulfilled on IC 309/2.2:

During the reference cycle, during the 11 ms pulse from single shot IC 304/2.2 pushbutton [31] 4 or [31] 5 depressed.

10.3.3.2.4. Charge, Recharge, TP 302, TP 304

The signal "charge" is generated in the meas.cycle for delay measurement in the period of "reset FF 2" and "100 ms release" by the clock pulse.

The signal "recharge" is generated in the reference cycle. A phase step generated by the line being tested causes the times "charge" and "recharge" in the meas. and reference cycles to be of different lengths. The difference is displayed as the result of the delay test

10.3.3.3. Indication Amplifier with Display Buffer

The indication amplifier evaluates the offered signals and displays them.It contains the measuring range switch for the group delay level and attenuation. In the case of group delay measurements the indication amplifier operates as a phase meter.

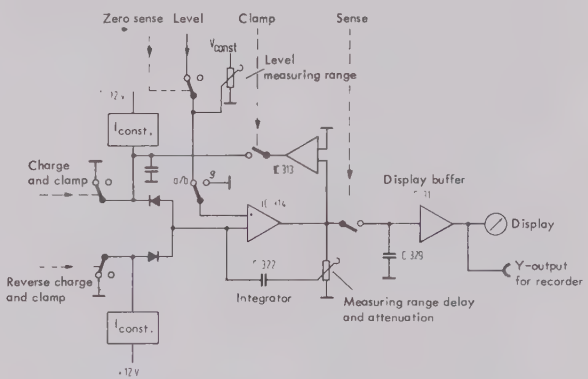

Figure 10-15 Basic circuit of the indication amplifier

10.3.3.3.1. Delay Measurements (Pushbutton [31] 3)

The phase meter consists basically of an integrator which is driven by two exactly equal currents of opposite polarity . Depending on which current flows for a longer period the result of measurement is either positive or negative, see Figure 10-16.

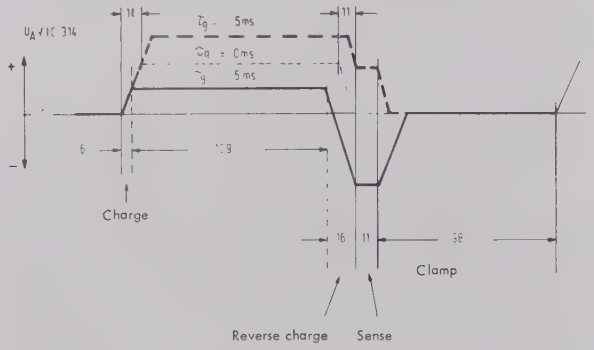

Figure 10-16 Charging, recharging, and sensing operation for various delays

The amplitude of the test result is determined by the period of the currents and by the size of the integration capacitor. In order to obtain a sufficient range of measurements the size of the integration capacitor can be selected by means of the range selection switch.

The signals "charge" and "recharge" control transistors T 306, T 310 for release of the negative and positive constant currents.

The positive current is determined by GL 306 (ZPD 5.1) and the resistors R 343 and P 301. If T 310 is cutoff during the recharging time the current flows via GL 308 to the integrator. The delay indication is aligned with potentiometer P301.

The negative current is determined by GL 305 and R 338. It is approximately 0.5 mA larger than the positive constant current. The regulation circuit ensures, during the clamping operation, that the superfluous current is drained to +12 V via R 337 and T 311.

The regulation circuit monitors the output voltage of the integrator (IC 314) and sets the output voltage of the integrator to 0 V during the clamping operation (T 317 conducting, T 306 and T 310 cutoff). After the loop is opened (T 317 cutoff) the current equality is maintained by the buffer effect of C 321 until the next clamping operation. A further task of the regulation circuit is to regulate the test results which occur in the rhythm of the 4.16 Hz signal during the 98 ms clamping time.

GL 314 and GL 315 are used for limiting the output voltage of IC 314. If this limiting action is activated then the output divider is no longer active and an integration constant for an amplification of 1 is the result.

With the aid of T 318 the test result is sensed for 11 ms immediately after recharging (sensing pulse) i.e. it is transferred to the display buffer C 329. The series resistor (R 384, R 385) can be switched with the aid of pushbutton [31] 6 to obtain either a "rapid" or a "slow" display. In the position "slow" it is thus possible to average out any noise.

Due to the different series resistors an increased offset of IC 316 must be expected in the switch position "slow". The offset for the two positions can be averaged with the aid of potentiometer P 304.

10.3.3.3.2. Absolute Level Measurement (Pushbutton [31] 5)

The indication amplifier receives the input signal from the amplitude channel via terminal 25. It is a DC voltage in the range +1 V to -5 V, corresponding to the input level range +10 dBm to -50 dBm

In order to prevent indication errors due to drift the zero point is calibrated in the rhythm of the 4.16 Hz signal. This is done by the clamping operation, similar to the delay measurement, whereby the regulation circuit (IC 313, T 317, T 311) is closed for a period of 11 ms.

Due to the zero sensing pulse (also 11 ms) which arrives simultaneously T 314 is cutoff and the reference side of the integrator (G_2 of T 312) is connected only to the wiper of switch [33] . A constant voltage which depends on the selected level measuring range is tapped off here from the divider R 382 to R 390.

This voltage forms the reference voltage for the centre scale position 0 dB on the meter [10] . A level measurement of ± 10 dB from this reference point is now possible. After the clamping operation the regulation circuit is interrupted (T 317 cutoff, T 306 and T 310 conducting) and T 314 conducts. The voltage coming from the amplitude channel now causes a shift of the reference voltage according to its amplitude and thus a corresponding output voltage at IC 314. The reference point obtained previously in the clamping operation remains stored in the integrator during the measuring operation.

The output voltage of IC 314 is sensed in the same manner as the delay measurement and transferred to the display buffer.

10.3.3.3.3. Attenuation Measurement (Pushbutton [31] 4)

In this measuring mode there is no zero sensing signal. Transistor T 414 conducts continuously.

During the clamping operation in the measuring cycle (see pulse diagram of receiver) the measured level is stored as a reference and the output voltage of IC 314 is sensed during the reference cycle. The output voltage now supplies the difference between the meas. and reference levels. As the meas. level is used as the reference the display of the attenuation has the correct polarity with respect to the reference level.

10. DESCRIPTION OF FUNCTION

The selection of the attenuation measuring range is carried out with switch (23) and its divider resistor R 391 to R 397.

10.3.3.3.4. Zero Calibration (Pushbutton 31 1)

With pushbutton 31 1 depressed the input of IC 316 is connected to ground via resistor R 379. At the same time pin 5 of IC 540 is connected to ground. The recorder outputs Bu 34 and Bu 35 of the receiver signals are now available for zero adjustment of the recorder.

10.3.3.3.5. Full Scale Calibration Pushbutton 31 2)

In this case a DC voltage which causes full scale deflection on the meter 10 and a voltage of +2.5 V at the recorder 34 is connected to the input of IC 316.

This voltage is adjusted with potentiometer P 303.

Pin 5 of IC 543 is open and the required frequency is connected to the 800 ns single shot IC 503 via IC 541/2.1.

The frequency 10 x $f_{nominal}$ is derived from the multivibrator IC 507/3.3 via IC 504/2.1 to IC 540. The input of the discriminator receives pulses from IC 540 which are proportional to the frequency. A DC voltage which is proportional to the frequency is generated in the discriminator and is available at socket Bu 35 of the receiver.

10.3.4. Frequency Evaluation (5)

10.3.4.1. AGC Amplifier

The AGC amplifier is intended to convert the possible level range at the input (-50 to +10 dBm) to a constant value so that frequency measurement of the input signal is possible within the range 200 Hz to 20 kHz. The following Schmitt trigger shapes the signal into a square-wave for further evaluation. The frequency of the input signal is designated $f_{nominal}$ in the circuit diagrams.

An internally generated frequency is adjusted to 10 x the value of this frequency.

$$f_{actual} = 10 \times f_{nominal}$$

The first partial amplifier (IC 501/2.1) receives part of the input signal from the input amplifier Ü 202. With an input level of 0 dBm a level of +3 dBm (≅ 1.1 V) is available at TP 501.

The AF voltage for the speech adapter is coupled out via T 505 and R 529.

The second partial amplifier (V = 66 dB) supplies the rectifier GL 501, 502. The AGC transistors T 501, T502 are controlled by the rectified voltage. The AGC effect is due to the fact that a level dependent division occurs between R 505 and the resistance via the emitters of T 501 and T 502. This AGC loop also stabilizes the working point. The output voltage of the AGC amplifier can be checked at TP 502.

Over the whole level range +10 to -50 dBm the output voltage remains constant in the range

$$V_{pp} = 4 \text{ to } 5 \text{ V}$$

The Schmitt trigger converts the sine-wave voltage into a square-wave voltage with V_{pp} = 5.6 V. The hysteresis of the Schmitt trigger is selected so that overlaid interference signals and the edge frequency modulation (which are not suppressed by the AGC amplifier) have no negative effects. The pulse duty cycle (D = 0.5) is adjusted with potentiometer P 501.

10.3.4.2. Difference Flip-Flop, Charging Circuit and Multivibrator

An internal oscillator (multivibrator) is synchronized to 10 x the value of the measuring or reference frequency only for a period of 50 ms. During the rest of the time the multivibrator runs freely at this frequency so that the frequency to be measured is always available to the frequency counter.

The frequency comparison and the storage of the AGC voltage are carried out by the difference flip-flop and the charge circuit.

10.3.4.2.1. Multivibrator

The frequency range of the a stable multivibrator is changed by a factor of 100 to 2 kHz to 200 kHz by changing the backward charging current. The backward charging current is a current obtained by means of the multivibrator control voltage T 510, T511 and R 579. Two emitter coupled transistors T 512, T 513 are used to sense the backward charging curve of C 545.

In order to ensure that the multivibrator starts GL 521 and T 514 check whether the multivibrator is oscillating. The feedback consists of GL 521, T 514, IC 510/6.6, IC 507/3.3 and generates via

C 547 a pulse which causes the multivibrator to start.

When the multivibrator is oscillating C 546 is charged positively, T 514 conducts continuously, and a zero signal is always present at input 5 of the OR circuit IC 507/3.3.

IC 507/3.3 is also used as a coupling element for the following difference flip-flop.

The AGC voltage at TP 503 is in the range +6V to +1 V for frequencies 200 Hz to 20 kHz.

The pulse stage IC 504/2.1 receives the multivibrator frequency $f_{act.}$ from 2 kHz to 200 kHz.

10.3.4.2.2. Difference Flip-Flop and Charge Circuit

The function of the difference flip-flop is basically the following: a pulse of the nominal frequency sets flip-flop IC 506/2.2 to state A, and the next pulse of the actual frequency sets it to state B. This is continued until two nominal frequency pulses or two actual frequency pulses arrive sequentially. In this case the second pulse is released by an AND circuit IC 511/4.4 or IC 508/2.2 and used for adjustment of the frequency. The difference frequency between $f_{act.}$ and $f_{nominal}$ appears at the outputs.

If two pulses arrive simultaneously at the difference flip-flop neither may be evaluated.

This is monitored by means of IC 507/3.1 and IC 506/2.1 inhibits the input of the difference flip-flop. The phase of the synchronized frequency beats until the pulses no longer overlap. After this the difference flip-flop is released again. Only every tenth pulse of the frequency $f_{act.}$ (2 to 200 kHz) may be evaluated and for this reason the frequency is divided in the ratio 10:1 via IC 509.

In order to ensure that the difference flip-flop receives sufficient clock pulses in all cases the clock pulses for IC 505/2.1 and IC 504/2.2 are shorter ($t_p \approx 500$ ns) than the pulses at IC 503 and IC 504/2.1, which observe an approach ($t_p \approx 800$ ns). The inhibit flip-flop (IC 506/2.1) is unlocked with each pulse of the actual or nominal frequency. This means that the 1st, 2nd, 3rd,..pulse of the actual frequency can perform the unlocking operation. After this, for example with the 2nd pulse, the difference flip-flop is released so that the 3rd to 10th pulses arrive at the output as correction pulses. These would however be false pulses. For this reason, after the inhibit, IC 538/2.2 prevents, on the basis of pulse overlap, the impulses 2-10 from reaching the output at TP 512. This means that only the 1st pulse is used for frequency correction.

The charge circuit following the difference flip-flop is dimensioned so that one charge pulse results in an output voltage variation corresponding to 1 kHz. If the frequency is very far from the required frequency (pulse sequence frequency > 10 Hz) adjustment is carried out at 10 x the speed (in the position "slow" by 1/10 Hz or 1 Hz in the case of large displacement). This means that a continuous signal can appear at the output if the frequency is greatly displaced; this is however permissible.

The switching of the steepness is carried out by means of the charge pulse period. For 0.1 Hz/pulse the output pulse (0.5 us) from the difference flip-flop is used and for 1 Hz/pulse the pulse which is extended to 5 us by means of IC 512/2.1. For 10 Hz/pulse the operating time of IC 512/2.1 is switched by means of IC 512/2.2.

In order to make the charging current for the charging independent of the IC output voltage the logical "0" is split off by diodes GL 515 and GL 516. Transistors T 507 and T 508 are connected as diodes. This results in leakage currents < 3 pA per transistor at 25°C and 0.3 V backward voltage. Preliminary integration of the charge pulses is carried out in C 538 and the main integration in C 539.

The control signal of the charging circuit for the multivibrator to be synchronized is available at TP 503.

10.3.5. Speech Adapter (6)

In order to permit universal use of the speech adapter this unit contains a cradle circuit. Its electrical data correspond to those of the "Ga 66" of the Federal German Post Office.

For approximately ideal compensation the simulation circuit is terminated with the same impedance as is found in two and four wire systems (600 Ohm).

10.3.5.1. Speech Operation

The cradle circuit has the task, for two wire operation, of connecting the combined microphone-loudspeaker and ear-piece and mouth-piece to the two wire line or, for four wire operation,

10. DESCRIPTION OF FUNCTION

o the match the two wire telephone to our wire line. The input signals from the microphone or speech unit are amplified in IC 602 and connected via divider P 605 to the four wire input of the cradle circuit. From the four wire output the AF signal is fed via IC 604, amplified in the power stage T 606, T 607 and drives the loudspeaker or ear-piece. The required operating mode (two wire input, two wire output or four wire) can be selected by means of pushbuttons 29 1 to 29 3. With pushbutton 29 1 depressed the two wire telephone connection is prepared for connection to the output socket Bu 2301. The two wire connection of the cradle circuit is switched to the position "speak" if the ear-piece and mouth-piece are used by contact S 603 on Bu 14 or by the strap 4-5 in the diode plug to socket 13 if a microphone is used. Socket 24 and the two wire connection of the cradle circuit are thus connected directly to the output socket Bu 2301. The receiver remains ready to receive due to the idle positions of the change-over contacts of pushbutton 29 2 (S 601/II).

The same is true in a similar manner for input socket Bu 201 when pushbutton 29 2 is depressed (S 601/II).

For four wire operation the two wire telephone connection at socket 24 is connected to the two wire connection of the cradle circuit by means of pushbutton 29 3. If the operating mode switch 22 is also set to the position "speak" then the four wire output and the microphone amplifier are connected to the output socket Bu 2301 via the output amplifier of the generator and the four wire input and the AF amplifier input (IC 604) are connected to the input amplifier of the receiver.

As the wiring of this circuit is rather complicated the two signal paths are shown below.

Four wire output: cradle circuit - S 601/II/a-S 604/II/b-output amplifier -Ü 2301-R_i Field-S 601/a + b-S 604/I/b-S 604/I/b and S 604/I/a-Bu 2301.

Four wire input: Bu 201-S 604/IV/b and S 604/IV/a-S 601/II/c-R_i Field-Ü 201-AGC Amplifier-T 505-S 601/I/c-IC 603-Cradle Circuit Four Wire Input and in parallel to this via S 601/I/c-P 601-AF Amplifier-Loudspeaker Lsp 601-ear-piece.

wo wire operation with pushbutton 29 1 depressed
The generator output is ready to receive speech signals and passes these via the decoupling stage for telephony to the loudspeaker.

Signal flow: Bu 2301-R_i Field-Ü 2301-T 2316-IC 2308-S 604/III/a-S 601/I/c-P 601-IC 604-Lsp 601.

If the test set is switched to receiver input by means of pushbutton 29 2 the receiver is always ready to receive speech signals.

The signal flow is as follows: Bu 201-S 604/IV/a + b-S 601/II/b + c-R_i Field-Input Amplifier-AGC Amplifier T 505-S 601/I/d-IC 603-S 601/I/c-P 601-IC 604-Lsp 601.

10.3.5.2. Automatic Volume Switching

If a signal modulated in accordance with CCITT is present at the receiver input then a 4.16 Hz square-wave signal with a period of 240 ms is present at pin (6) 1 of the speech adapter. A 230 ms single shot T 601, T 602 is started by this signal and a 20 ms single shot T 604, T 605 is started when the 230 ms have elapsed. If a trigger pulse for the 230 ms single shot arrives during the running time of the 20 ms single shot then a clock pulse for counter IC 605 is generated. After eight sequential clock pulses the output pin 8 of the counter switches to "zero" then cuts off T 608. In addition further clock pulses are prevented by IC 601/4.4 so that the zero signal remains present at pin 8.

This reduces the amplification factor of the AF amplifier and reduces the volume at the loudspeaker. If on the other hand a clock pulse arrives outside the 20 ms operating time - this is the case with speech modulation from the receiver input - the counter is reset and the loudspeaker is switched "loud". P 603 on the 230 ms single shot is adjusted so that the clock pulse arrives exactly in the centre of the 20 ms operating time in the case of a 240 ms signal.

10.3.5.3. AF Amplifier, Microphone Amplifier

The AF Amplifier consists of IC 604 and a complementary output stage T 606, T 607. The AC voltage amplification is 20 dB and is determined by the divider ratio R 632 and R 626. The isolating amplifier IC 603 decouples the receiver output from the cradle circuit. The switchable divider for automatic volume switching is located at its input. The microphone amplifier IC 602 has an adjustable amplification (10-207 x).

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10.4. POWER SUPPLY UNIT ①

The regulation power supply unit generates the operating voltages +12 V -12 V +5 V and a stabilized voltage of +6.5 V. The mains side of the transformer and the protective conductor are fitted with chokes to reduce radio frequency interference.

The mains voltage can be selected by means of the mains voltage selection switch.

All three regulation circuits are constructed in accordance with the same principle. The main differences are in the dimensioning.

The regulation circuit of the +12 V supply voltage is described as an example.

The voltage from the secondary side of the mains transformer is fed via a protective resistor to rectifier GL 101. The DC voltage is smoothed on capacitor C 101 and is passed to the control element transistor T 101 and to IC 101 pins 7 and 8. IC 101 carries out an actual/nominal value comparison in order to control the control element T 101 accordingly. The required voltage is set up with potentiometer P 102. The actual value corresponds to the +12 V supply. The power supply unit is short circuit proof, the current limiting circuit with R 124 R 125 and R 108 protecting the control transistor from thermal overload when the output is short circuited.

An auxiliary supply is provided from the output of the +12 V supply voltage for the regulation circuit of the -12 V supply voltage.

A +6.5 V operating voltage is necessary for the frequency display. It is generated by the cascade circuit with C 103 and C 104. The +6.5 V voltage is stabilized at the output of the +5 V supply voltage. The cascade circuit with T 107 T 106 and T 105 is controlled by divider R 144, R 145.

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